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3 **QSFP-DD MSA**
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6 **QSFP-DD/QSFP-DD800/QSFP-DD1600 Hardware Specification**
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8 **for**
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10 **QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVERS**
11
12
13 **Revision 7.1**
14
15
16 **June 25, 2024**
17
18

19 Abstract: This specification defines: the electrical and optical connectors, electrical signals and power supplies,
20 mechanical and thermal requirements of the pluggable QSFP Double Density (QSFP-DD/QSFP-DD800/QSFP-
21 DD1600) connector and cage system. QSFP-DD MSA family of modules and cages remain fully backward
22 compatible with the classic QSFP+ formfactor. This document provides a common specification for systems
23 manufacturers, system integrators, and suppliers of modules.
24
25
26 **POINTS OF CONTACT:**

Ali Ghiasi (Technical Editor)
Ghiasi Quantum
19947 Lindenbrook Lane
Cupertino, CA 95014
ali at ghiasiquantum dot com

Mark Nowell (Co-Chair)
Cisco
170 West Tasman Dr
San Jose, CA 95134
mnowell at cisco dot com

Scott Sommers (Co-Chair)
Molex
2222 Wellington Court
Lisle, IL 60532-1682
scott.sommers at molex dot com

27
28 **Website:**
29 www.QSFP-DD.com
30

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45

1 **Dedication:**
2 The members of the QSFP-DD MSA would like to acknowledge the contributions of Mr. Edmund Poh. He was
3 an excellent engineer; his technical skills and collaborative attitude will be missed.
4
5 The following are Promoter member companies of the QSFP-DD MSA.

Broadcom	Foxconn Interconnect Technology	Lumentum
Cisco	Huawei	Nvidia
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Coherent	Juniper Networks	TE Connectivity

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7 The following are contributing member companies of the QSFP-DD MSA.

Accelink	Hakusan	Nokia
ACON	Hewlett Packard Enterprise	Panduit
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Fujitsu Optical Components	NEC Corporation	Yamaichi
Genesis Connected Solutions		

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9

1
2 **Change History:**

Revision	Date	Changes
1.0	Sept 19, 2016	First public release
2.0	March 13, 2017	Second public release
3.0	Sept 19, 2017	Third public release
4.0	Sept 18, 2018	Fourth public release, Additions of thermal section, synchronous clocking in 4.9, Mechanical updates.
5.0	July 9, 2019	Fifth public release, Added Module type 2A, changes to latch and cage drawings, added ePPS contact, updated power supply testing, added BiDi optical port assignments.
5.1	August 7, 2020	6th public release, Chapter 7-Management Interface is now part of CMIS [5]. Port mapping, optical connectors, and module color coding moved into a new Chapter 5.
6.0	May 20, 2021	7th public release, chapters for QSFP-DD800 and QSFP112 Mechanical and Board Definitions are added. Chapter for QSFP112 Electrical and management timing added. Updated power supply test method. Module power contacts rating increased from 1 A to 1.5 A and max module power dissipation increased to at least 25 W. Programmable/Vendor specifics and ePPS/Clock contacts defined. Normative connector performance Appendix A added.
6.01	May 28, 2021	8th public release, reinstated text inadvertently deleted in PCB notes in section 6.3 and 7.3, inadvertent change to a dimension in Figure 45 corrected.
6.2	March 11, 2022	9th public release, defined a new improved power supply test method, squelch level reduced to 50 mV for 112G operation, press hole separation increased to 3.1 mm in Figure 68. TWI bus timing removed from chapter 4 as identical timing diagram already included in CMIS [5].
6.3	July 26, 2022	10th public release, updated termination definition for P/VSx and ePPS/Clock signals, Figure 51 bezel opening height adjusted for consistency, updated Figure 75 glue zone.
7.0	Sept. 29, 2023	QSFP112 specifications were forwarded to SFF SNIA and are removed from this specifications, see [35] and [36]. Missing ModSelL signal is added to the QSFP-DD example circuit. QSFP-DD1600 mechanical specifications defined in chapter 8. Current rating for each of QSFP-DD1600 contacts are increased to 2 A with feasibility of at least 40 W module power dissipation. Appendix F defines QSFP-DD1600 enhanced thermal design with bottom heat sink.
7.1	June 25, 2024	Updated module noise output measurement, see 4.7.5. Added alternate method to test module noise tolerance, see 4.7.7. Figure 63 module stop changed to 3.6 mm. New improved paddle card design for QSFP-DD1600, see 8.3. New 2x1 QSFP-DD1600 cage system, see 8.5. Added optional high power module monitoring approach, see 9.4. QSFP-DD1600 module 2C defined, see Appendix C.

3
4 **Foreword**
5 The development work on this specification was done by the QSFP-DD MSA, an industry group. The
6 membership of the committee since its formation on Feb 2016 has included a mix of companies which are
7 leaders across the industry.
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1 Scope

The scope of this specification is the definition of high-speed/density 4 and 8 electrical lanes (4x, 8x) modules, cage and connector system. The QSFP-DD supports up to 400 Gb/s in aggregate respectively over 8 lanes of 50 Gb/s and over 4 lanes of 100 Gb/s electrical interfaces. The QSFP-DD800 supports up to 800 Gb/s in aggregate over 8 lanes of 100 Gb/s electrical interface. The QSFP-DD1600 supports up to 1600 Gb/s in aggregate over 8 lanes of 200 Gb/s electrical interface. The QSFP-DD/QSFP-DD800 cage and connector designs with 8 lanes are compatible with the 4 lanes QSFP+. The QSFP-DD1600 cage and connector is an incremental design with enhanced signal integrity and thermal which is backwards compatible to 8 lanes QSFP-DD and 4 lanes QSFP+. The QSFP-DD800 supports up to 112 Gb/s (56 GBd) per lane electrical operation based on PAM4 signaling and is expected to be compliant to IEEE 802.3ck [15] and OIF 112G-VSR [21]. The QSFP-DD1600 supports up to 224 Gb/s (112 GBd) per lane electrical operation based on PAM4 signaling and is expected to be compliant to IEEE 802.3dj [15] and OIF 224G-VSR [21] when published.

This specification is intended to be used in combination with the Common Management Interface Specification (CMIS) [5]. Mutual dependencies exist between these two documents for timing parameters, management interface and register specifications.

1.1 Description of Chapters

QSFP-DD/QSFP-DD800/QSFP-DD1600 specifications are organized in to 9 chapters and 5 appendixes addressing electrical/management, optical, mechanical, and environmental aspect of the module.

All the requirements shall be considered for both QSFP-DD, QSFP-DD800, QSFP-DD1600 unless otherwise specified, 6.1, 6.2, 6.3, 6.4 are mechanical foundation sections applicable to QSFP-DD/QSFP-DD800/QSFP-DD1600.

- Chapter 1 Scope and Purpose
- Chapter 2 References, Related Standards, and SFF Specifications
- Chapter 3 Introduction
- Chapter 4 QSFP-DD/QSFP-DD800/QSFP-DD1600 Electrical Specifications and Management Interface
- Chapter 5 Optical Port Mapping and Optical Interfaces
- Chapter 6 Mechanical specifications and printed circuit board definition for QSFP-DD
- Chapter 7 Mechanical specifications and printed circuit board definition for QSFP-DD800
- Chapter 8 Mechanical specifications and printed circuit board definition for QSFP-DD1600
- Chapter 9 Environmental and thermal considerations.
- Appendix A Normative Module and Connector performance requirements
- Appendix B Informative overall module length with elastomeric handle
- Appendix C Informative QSFP-DD/QSFP-DD800 Module Type 2A and 2B Heat Sink Examples
- Appendix D QSFP-DD800 Cage and Heat Sink Mechanism and EMI fingers
- Appendix E Informative QSFP-DD800 2x1 Cabled Connector and Cage
- Appendix F QSFP-DD1600 mechanical enhancements for high power modules.

2 References and Acronyms

2.1 Reference Standards and Specifications

The following documents are relevant to this specification:

[1] ANSI FC-PI-6 32GFC
[2] ANSI FC-PI-7 64GFC
[3] ANSI FC-PI-8 128GFC
[4] ASME Y14.5-2009 Dimensioning and Tolerancing
[5] Common Management Interface Specification (CMIS) 5.2, see https://www.oiforum.com/wp-content/uploads/OIF-CMIS-05.2.pdf
[6] EIA-364-1000 TS-1000B Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Controlled Environment Applications, revision B 2009
[7] EN6100-4-2 (IEC immunity standard on ESD), criterion B test specification
[8] Human Body Model per ANSI/ESDA/JEDEC JS-001
[9] IEC/UL 60950-1 Requirements for Information Technology Equipment, Section 4.5.4 (Touch Temperature Reference)
[10] IEC 61754-7-1 (Fibre Optic Interconnecting Devices and Passive Components - Fibre Optic Connector Interfaces - Part 7-1: Type MPO Connector Family - One Fibre Row)
[11] IEC 61754-7-2 (Fibre Optic Interconnecting Devices and Passive Components - Fibre Optic Connector Interfaces - Part 7-2: Type MPO Connector Family - Two Fibre Rows)
[12] IEC 61754-7-3 (Fibre Optic Interconnecting Devices and Passive Components - Fibre Optic Connector Interfaces - Part 7-3: Type MPO Connector Family - Two Fibre Rows 16 Fibre Wide)
[13] IEC 61754-20 (Fibre Optic Interconnecting Devices and Passive Components - Fibre Optic Connector Interfaces - Part 20: Type LC Connector Family)
[14] IEEE Std 802.3™-2022
[15] IEEE Std 802.3ck (100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces)
[16] IEEE Std 802.3dj (200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet interfaces)
[17] IEEE Std 1588 Precision Clock Synchronization Protocol PTP, 2019
[18] InfiniBand Architecture Specification Volume 2
[19] JEDEC JESD8C.01 Interface Standard for Nominal 3.0/3.3 V Supply Digital Integrated Circuit (LVCMOS)
[20] NXP UM10204, I2C-bus specification and user manual, Rev 7.0, October 2021.
[21] OIF CEI 5.1, CL-13 CEI-28G-VSR, CL-16 CEI-56G-VSR PAM4, and CL-25 CEI-112G-VSR PAM4 specifications
[22] SN-60092019 SN optical connector and receptacle, see http://www.qsfp-dd.com/optical-connector/
[23] Telcordia GR63 NEBSTM Requirements: Physical Protection, Section 4.1.7, December 2017
[24] TIA-604-5 (FOCIS 5 Fiber Optic Connector Intermateability Standard- Type MPO)
[25] TIA-604-10 (FOCIS 10 Fiber Optic Connector Intermateability Standard- Type LC)
[26] TIA-604-18 (FOCIS 18 Fiber Optic Connector Intermateability Standard- Type MPO-16) Interfaces - Part 7-1: Type MPO Connector Family - One Fibre Row)
[27] TIA-604-19 (FOCIS 19 Fiber Optic Connector Intermateability Standard- Type Sen Connector)
[28] USC-11383001 MDC optical plug and receptacle, see http://www.qsfp-dd.com/optical-connector/
[29] P2124A Injector Probe - https://www.picotest.com/product/p2124a
[30] Measuring PSNR/PSRR/PSMR to meet QSFP/OSFP high-speed Requirements", Steve Sandler, Bob Tarasewicz, Pavel Zivny, Tony Ambrose, DesignCon 2023
[31] Power Integrity Testing Requirements Introduce Extreme Interconnect Measures", Steve Sander, Signal Integrity Journal, February 2023.

2.2 SFF Specifications:

[32] SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface, Rev. 4.1
[33] SFF-8636 Management Interface for Cabled Environments, Rev. 2.11
[34] SFF-8661 Specification for QSFP+ 4X Module, Rev. 2.5
[35] SFF-8679 QSFP+ 4X Hardware and Electrical Specification, Rev. 1.8
[36] SFF-TA-1027 QSFP2 Cage, Connector, & Module Specification, Rev. 1.0.

2.3 Acronyms and abbreviations

The following acronyms may be used in this specification.
ASIC - Application Specific Integrated Circuit
CDR - Clock and Data Recovery
CMIS – Common Management Interface Specifications
DCR – DC Resistance
DSP – Digital Signal Processing
EMI - Electromagnetic Interference
ESD - Electrostatic Discharge
ESR - Equivalent Series Resistance
Gb/s - Gigabits per second
GBd – Gigabaud
HCB - Host Compliance Board
IntL – Interrupt on Low Transition
I/O – Input/Output
LOS – Loss of Signal
LVCMOS - Low Voltage Complementary Metal Oxide Semiconductor
LVTTL - Low Voltage Transistor-Transistor Logic
MCB - Module Compliance Board
NEBS - Network Equipment Building System
OMA - Optical Modulation Amplitude
PAM – Pulse Amplitude Modulation
PCB - Printed Circuit Board
PPS – Pulse Per Seconds
PSU – Power Supply Unit
PSNR – Power Supply Noise Rejection
PTP – Precision Time Protocol
Rx – Receive Lanes
Retimer – A device that uses a recovered clock to retime the data also referred to as a CDR
SerDes - Serializer-Deserializer
SMT – Surface Mount Technology
TIA – Transimpedance Amplifier
TTL – Transistor-Transistor Logic
Tx – Transmit Lanes
TWI – Two wire interface compatible with NXP I^{2}C [20].

2.4 Document Source

The QSFP-DD/QSFP-DD800/QSFP-DD1600 Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER can be obtained via the www.QSFP-DD.com web site.

3 Introduction

This Specification covers the following items:

a) Electrical interfaces including pad assignments for data, control, status and power supplies and host PCB layout requirements.

b) Optical interfaces (including optical receptacles and mating fiber plugs for multimode and single-mode duplex and parallel fiber applications). Breakout cable applications are also specified. Optical signaling specifications are not included in this document but are defined in the applicable industry standards.

c) Mechanical specifications including dimensions and tolerances for the connector, cage and module system. Includes details of the requirements for correct mating of the module and host sides of the connector.

d) Thermal requirements

e) Electrostatic discharge (ESD) requirements by reference to industry standard limits and test methods.

f) Timing requirements for management interface, low speed I/O, soft control and status functions.

This Specification does not cover the following items:

a) Electromagnetic interference (EMI) protection. EMI protection is the responsibility of the implementers of the cages and modules.

b) Common memory map definition, which can be found in the 'Common Management Interface Specification for 8x/16x pluggable transceivers' [5].

3.1 Document Overview and Organization

Implementations compliant to electrical signal contact and lane assignments, electrical and power requirements for QSFP-DD/QSFP-DD800/QSFP-DD1600 are defined in Chapter 4. The optical lane assignments are defined in Chapter 5 ensure that the pluggable modules and cable assemblies are functionally interchangeable. Dimensions, mounting and insertion requirements defined in Chapter 6 for the bezel, optical module, cable plug, cage and connector system on a circuit board ensure that these products are mechanically interchangeable. Chapter 7 describes an improved QSFP-DD form factor called QSFP-DD800 with improved signal integrity for 100 Gb/s (56 GBd) per lane operation with an aggregate bandwidth of 800 Gb/s. Chapter 8 describes an improved QSFP-DD form factor called QSFP-DD1600 with improved signal integrity for 200 Gb/s (112 GBd) per lane operation with an aggregate bandwidth of 1.6 Tb. Environmental and thermal considerations are defined in Chapter 9.

Normative connector performance tables are in Appendix A, informative module overall length in Appendix B, informative QSFP-DD/QSFP-DD800 module type 2A/2B heat sink examples in Appendix C, informative QSFP-DD800 cage, heat sink, and EMI fingers in Appendix D, informative QSFP-DD800 2x1 cabled connector and cage system in Appendix E, and QSFP-DD1600 mechanical enhancements for high power modules in Appendix F.

3.2 Applications

This specification defines an eight-lanes and four-lanes pluggable modules (including cables) which may satisfy e.g., Ethernet, InfiniBand, and/or Fibre Channel requirements. The QSFP-DD/QSFP-DD800/QSFP-DD1600 specifications are applicable to pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper wires. QSFP-DD/QSFP-DD800/QSFP application reference model is shown in Figure 1, where the focus of this specification is mechanical, electrical and thermal behavior at the interface between a host and the QSFP-DD/QSFP-DD800/QSFP-DD1600 modules.

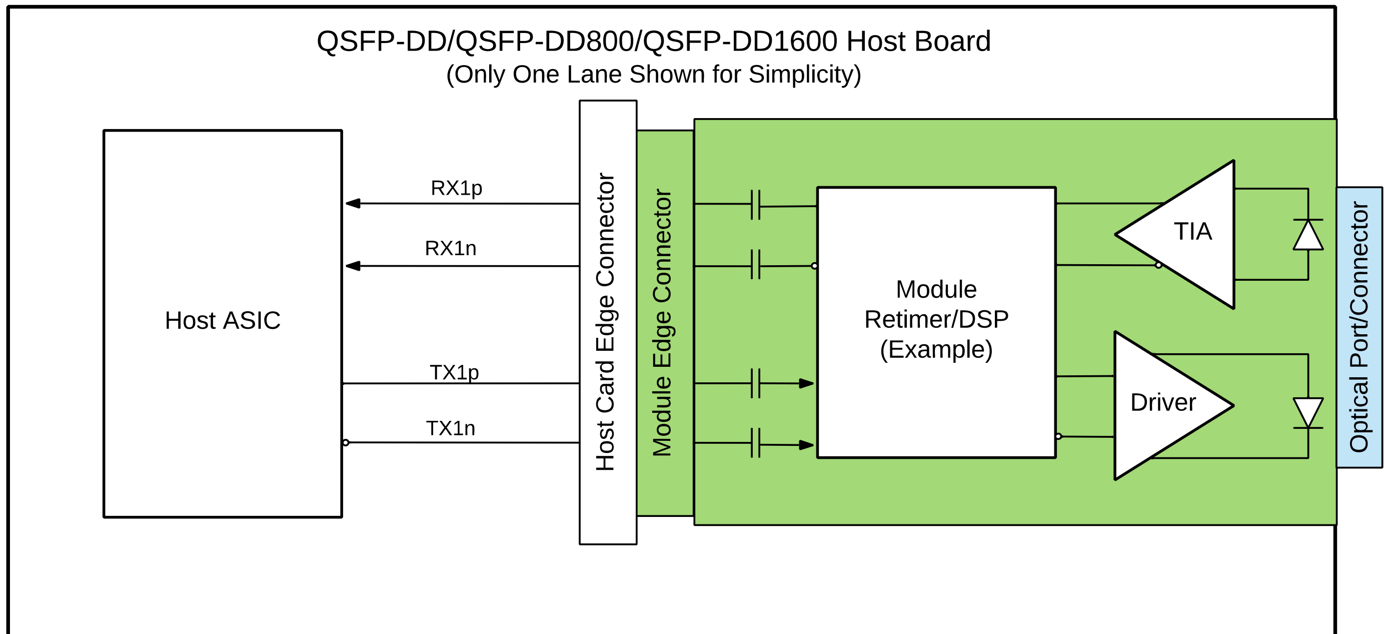


Figure 1: Application Reference Model

Note: For high speed electrical signals and compliance board methodology for 50-200 Gb/s/lane C2M operation see IEEE 802.3 clause 120E [14], IEEE 802.3ck clause 120G [15], and IEEE 802.3dj 200 Gb/s/lane [16], OIF CEI-56G-VSR-PAM4 and OIF CEI-112G-VSR [21]. For high-speed copper cabling see IEEE 802.3ck CL 162 [15].

3.3 Module management and control

The CMIS memory management map is defined for QSFP-DD, QSFP-DD800, and QSFP-DD1600 module management and control. Note: The CMIS management memory map structurally supports multiples of 8 lanes. In case of QSFP+ module plugged into QSFP-DD/QSFP-DD800/QSFP-DD1600 socket, host lanes 5-8 are physically not connected and should be ignored. The QSFP+ module makes use of host lanes 1-4 only.

1

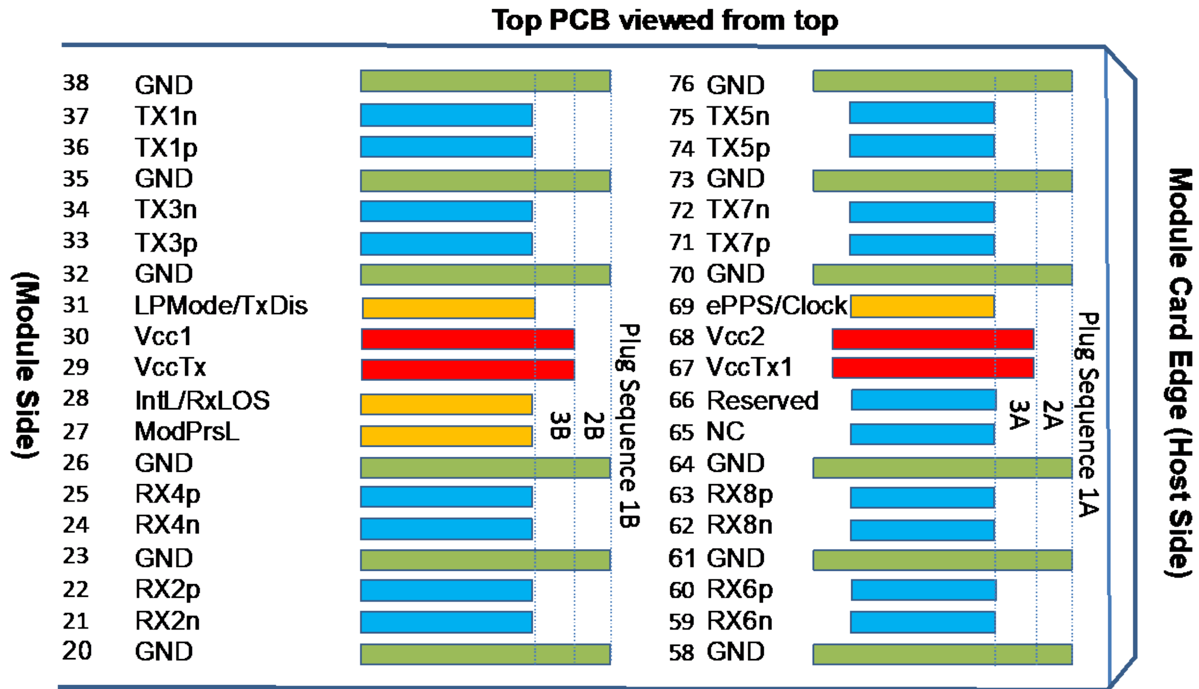
2 # 4 QSFP-DD Formfactor Electrical and Management Interface Specifications

3 This chapter contains signal definitions and requirements of QSFP-DD/QSFP-DD800/QSFP-DD1600 modules.
4 High-speed signal requirements including compliance points for electrical measurements are defined in the
5 applicable industry standards. Host designed to the requirement of this chapter accept modules in the QSFP+
6 family as well as QSFP-DD/QSFP-DD800/QSFP-DD1600 modules.
7

8 ## 4.1 Electrical Connector

9 The QSFP-DD/QSFP-DD800/QSFP-DD1600 module edge connector consists of a single paddle card with 38
10 pads on the top and 38 pads on the bottom of the paddle card for a total of 76 pads. The pads are defined in
11 such a manner to accommodate insertion of a classic QSFP+ module into a QSFP-DD/QSFP-DD800/QSFP-
12 DD1600 receptacles. The classic QSFP+ signal locations are deeper on the paddlecard, so that classic
13 QSFP+ module pads only connect to the longer row of connector pads, leaving the short row of connector
14 pads unconnected in a QSFP+ applications.
15
16 The pads are designed for a sequenced mating:
17
18 First mate “1A/1B”– ground pads
19 Second mate “2A/2B”– power pads
20 Third mate “3A/3B”– signal pads
21
22 Where color green identifies ground pads, color red identifies power pads, color orange identifies low speed
23 signal/control pads, and color blue identifies high speed I/O pads.
24
25 Because the QSFP-DD/QSFP-DD800/QSFP-DD1600 modules have 2 rows of pads, the additional QSFP-
26 DD/QSFP-DD800 pads will have an intermittent connection with the classic QSFP+ pads in the connector
27 during the module insertion and removal. The 'classic' QSFP+ pads have a 'B' label shown in Table 1 to
28 designate them as the second row of module pads to contact the QSFP-DD/QSFP-DD800/QSFP-DD1600
29 connectors. The additional QSFP-DD/QSFP-DD800/QSFP-DD1600 pads have an 'A' label in Table 1 to
30 designate them as the first row of module pads to contact the QSFP-DD/QSFP-DD800/QSFP-DD1600
31 connectors.
32
33 The additional QSFP-DD/QSFP-DD800/QSFP-DD1600 pads have first, second and third mate to the
34 connector pads for both insertion and removal. Each of the first, second and third mate connections of the
35 classic QSFP+ pads and the respective additional QSFP-DD/QSFP-DD800/QSFP-DD1600 pads are
36 simultaneous.
37
38 Figure 2 shows the signal symbols and pad numbering for the QSFP-DD/QSFP-DD800/QSFP-DD1600 module
39 edge connectors. The diagram shows the module PCB edge as a top and bottom view. There are 76 pads
40 intended for high speed signals, low speed signals, power and ground connections.
41
42 Table 1 provides more information about each of the 76 pads. Figure 45 and Figure 46 show QSFP-DD pad
43 dimensions and Figure 66 and Figure 67 show QSFP-DD800 pad dimensions. The QSFP-DD connector can
44 be integrated into a 2x1 stacked configuration with 2 ports as illustrated in Figure 47 Figure 32or a surface
45 mount configuration as shown in Figure 35. The QSFP-DD800 connector can be integrated into a 2x1 stacked
46 SMT configuration with 2 ports as illustrated in Figure 69, Figure 32 a surface mount configuration which is
47 identical to QSFP-DD 1x1 SMT as shown in Figure 35, and a 2x1 cabled connector cage system as shown by
48 Figure 108. The QSFP-DD1600 improved 1x1 SMT connector/cage is shown in Figure 82.
49
50 For EMI protection the signals from the host connector should be shut off when the QSFP-DD/QSFP-
51 DD800/QSFP-DD1600 modules are not present. Standard board layout practices such as connections to Vcc

and GND with vias, use of short and equal-length differential signal lines are recommended. The chassis ground (case common) of the QSFP-DD/QSFP-DD800/QSFP-DD1600 modules should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.



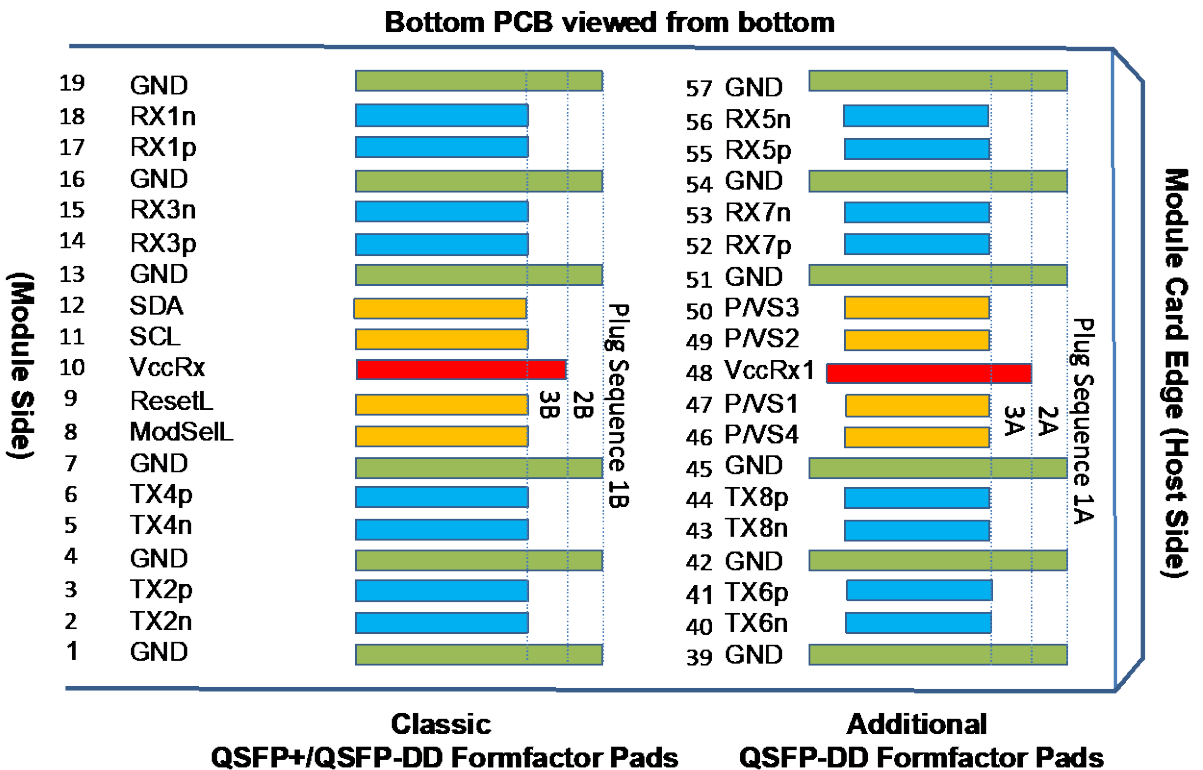


Figure 2: Module pad assignment and layout

1

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	TWI serial interface clock	3B	
12	LVCMOS-I/O	SDA	TWI serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1

2
3

1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000 mA.

Note 3: Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.

Note 6: for host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module see 4.2.6.

4.2 Low Speed Electrical Hardware Signals

In addition to the TWI serial interface the module has the following low speed signals for control and status:

- ModSelL
- ResetL
- LPMode/TxDis
- ModPrsL
- IntL/RxLOSL
- P/VS1, P/VS2, P/VS3, and P/VS4.
- ePPS/Clock

4.2.1 ModSelL

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD/QSFP-DD800/QSFP-DD1600 modules (see Table 7). When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP-DD/QSFP-DD800 modules on a single TWI interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any TWI interface communication from the host.

In order to avoid conflicts, the host system shall not attempt TWI interface communications within the ModSelL de-assert time after any QSFP-DD/QSFP-DD800/QSFP-DD1600 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4.2.2 ResetL

The ResetL signal shall be pulled to Vcc in the module (see Table 7). A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 9) initiates a complete module reset, returning all user module settings to their default state.

4.2.3 LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI interface except during the execution of a reset. Timing requirements for LPMode/TxDis mode changes are found in Table 9. LPMode is used in the control of the module power mode, see CMIS [5] Chapter 6.3.1.3.

When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits the host controls how much power a module can consume. When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters within the times specified in Table 9.

Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters. Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.

Note that the “soft” functions of TxDis, LPMode, IntL and RxLOSL allow the host to poll or set these values over the TWI interface as an alternative to monitoring/setting signal values. Asserting either the “hardware” or “soft bit” (or both) for TxDis or LPMode results in that function being asserted.

Editor's Note: registers to support optional TxDis will be added in future revisions of CMIS.

4.2.4 ModPrsL

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module (see Table 7). The ModPrsL is asserted "Low" when the module is inserted. The ModPrsL is deasserted "High" when the module is physically absent from the host connector due to the pull-up resistor on the host board.

4.2.5 IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board (see Table 7). At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI interface except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. "high" indicates that there is no loss of received optical power. Timing requirements for IntL/RxLOSL including fast RxLOS mode are found in Table 9. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.

Editor's note: registers to support optional RxLOSL will be added in future revisions of CMIS.

4.2.6 Programmable/Vendor Specific (Optional)

QSFP-DD MSA provides 2 input programmable/vendor specific pads (P/VS1, P/VS4) and 2 output programable/vendor specific pads (P/VS2, P/VS3). Programmable use case also includes vendor proprietary applications. P/VSx I/O are disabled by default.

Editor's Note - Logic definitions and programmable use cases for P/VSx input/output pads expect to be defined by QSFP-DD HW MSA and CMIS.

4.2.7 ePPS/Clock PTP Reference Clock (Optional)

Host ePPS/Clock The ePPS/Clock input is a programable timing and clock input, that can support unmodulated 1PPS (1 pulse per second), modulated 1PPS, and reference clock. The ePPS/clock is a LVCMOS compatible signal with series termination (TBD) on the host board and a parallel termination of at least 4.7 kΩ in the module. To improve signal integrity for faster clocks (i.e., 156.25 MHz) the parallel termination can be reduced to as low as 470 Ω and optionally AC coupled.

For high-performance Precision Time Protocol (PTP) applications, the ePPS (Enhanced Pulse Per Second) reference either with 1PPS modulated or unmodulated may be provided from the host to the module for time synchronization, see Table 2 for advertise capability. This can be used for either offline delay characterization or real-time delay compensation within the module. The ePPS is used to synchronize tightly the Host Time-of-Day counter to the module internal Time-of-Day Counter.

The ePPS/Clock module input optionally can be configured to provide reference clock to the CDR/DSP, see Table 2 for advertise capability.

Table 2- ePPS/Clock Advertising Capabilities

CMIS Byte Location (TBD)	Bit	Mode Supported
xxxxxx--	00	ePPS/Clock not supported
xxxxxx--	01	ePPS/Clock module supports either 1PPS mode, modulated 1PPS, or clock input for encoding see Table 3
xxxxxx--	10	ePPS/Clock supported TOD (Time of Day)
xxxxxx--	11	ePPS/Clock - Reserved

Table 3- ePPS or Clock Modes

CMIS Byte Location (TBD)	Bit	Mode Supported
xxxx--xx	00	RF clock for frequency see table y
xxxx--xx	01	1PPS send as unmodulated pulse duration TBD
xxxx--xx	10	1PPS send as 75%/25% duty cycle on RF modulated clock, for clock frequency see Table 4
xxxx--xx	11	ePPS/Clock - Reserved

Table 4- ePPS or Clock Frequency

CMIS Byte Location (TBD)	Bit	Mode Supported
----xxxx	0000	10 MHz
----xxxx	0001	12.5 MHz
----xxxx	0010	20 MHz
----xxxx	0011	24.576 MHz
----xxxx	0100	25 MHz
----xxxx	0101	156.25 MHz
----xxxx	0110-1101	Reserved
----xxxx	1110-1111	Custom

Editor’s Note: registers to support optional ePPS/Clock will be added in future revisions of CMIS.

1
2 **Table 5- Module ePPS/Clock Status Reporting (Required if module supports ePPS/Clock)**

CMIS Byte Location (TBD)	Bit	Mode Supported
xxxx--xx	00	ePPS/Clock signals not detected
xxxx--xx	01	1PPS unmodulated signal detected
xxxx--xx	10	1PPS modulated signal detected
xxxx--xx	11	Clock signal detected

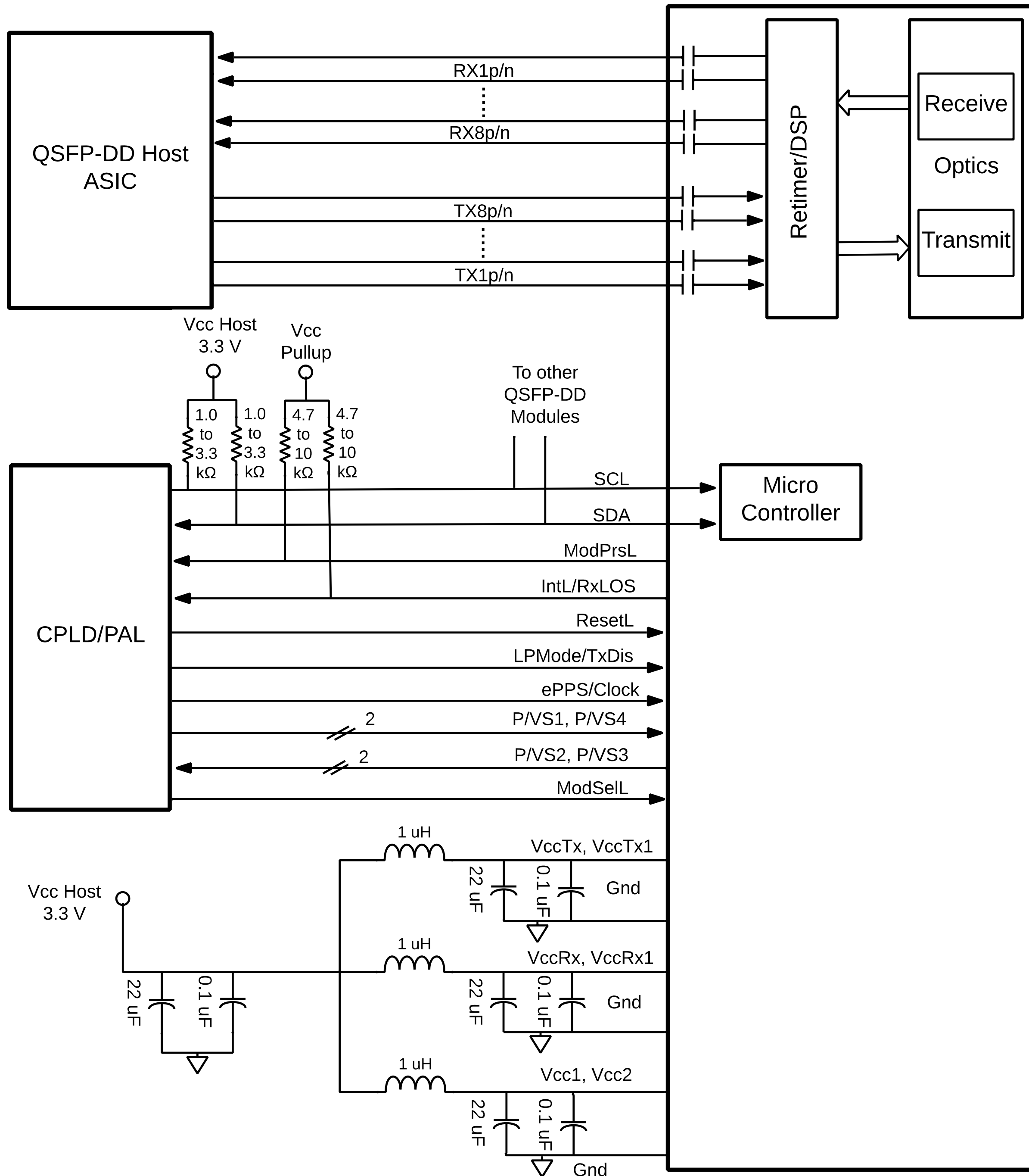
3
4 **Table 6- ePPS RF or Clock Frequency Reporting (Optional)**

CMIS Byte Location (TBD)	Bit	Mode Supported
----xxxx	0000	10 MHz (ePPS RF)
----xxxx	0001	12.5 MHz (ePPS RF)
----xxxx	0010	20 MHz (ePPS RF)
----xxxx	0011	24.576 MHz (ePPS RF)
----xxxx	0100	25 MHz (ePPS RF)
----xxxx	0101	156.25 MHz (Clock)
----xxxx	0110-1101	Reserved
----xxxx	1110-1111	Custom

5
6

7 4.3 Examples of QSFP-DD Module Formfactor Host Board Schematic

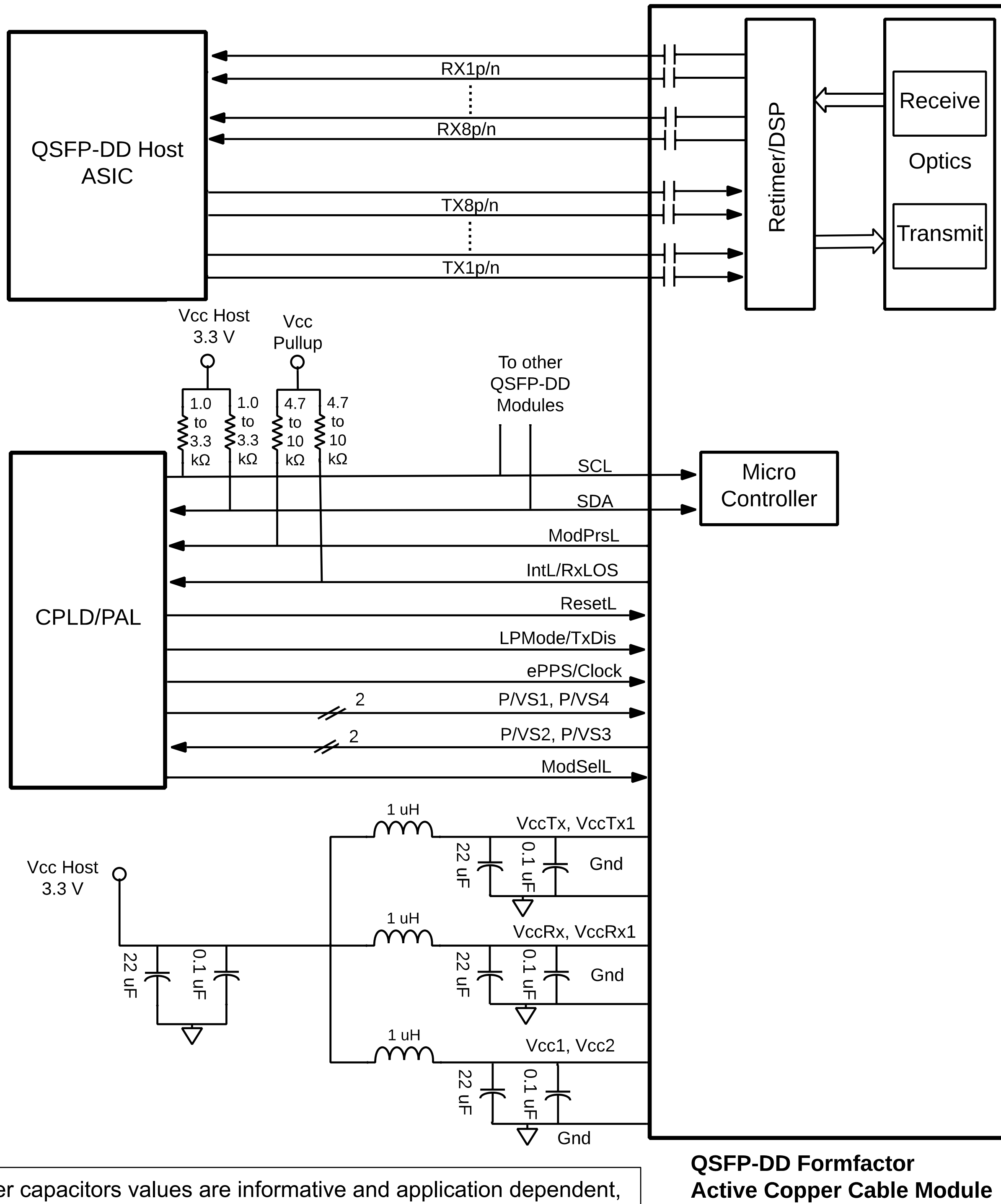
8 Figure 3, Figure 4, and Figure 5 show examples of QSFP-DD/QSFP-DD800/QSFP-DD1600 host PCB
9 schematics with connections to CDR and control ICs. An 8-wide electrical/optical interface is shown. Note
10 alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.
11



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

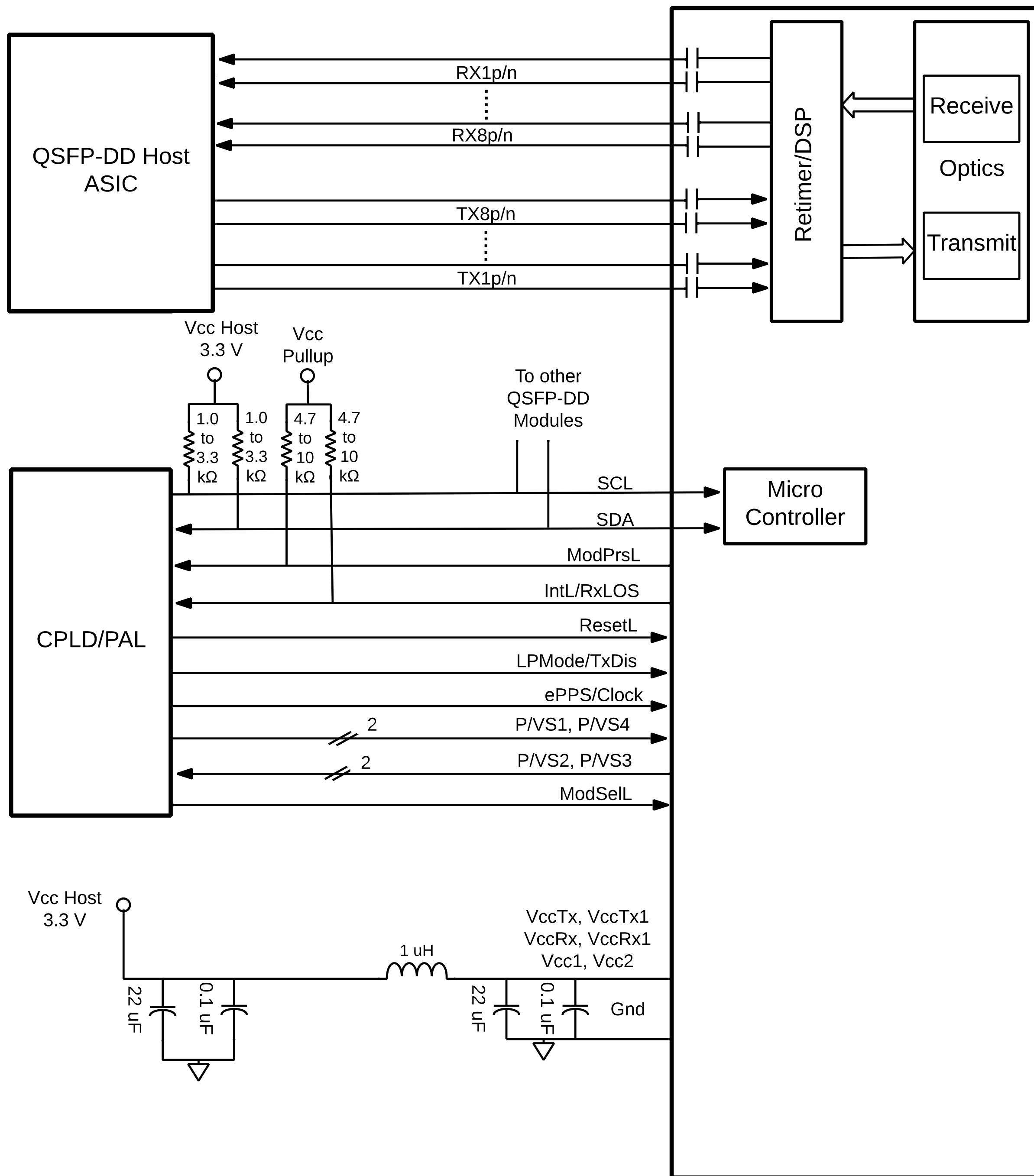
Figure 3: Example QSFP-DD host board schematic for Optical Modules



Note: Filter capacitors values are informative and application dependent, 0.1 μF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

Figure 4: Example QSFP-DD host board schematic for Active Copper Cables Module



QSFP-DD Formfactor
Passive Copper Cable Module

Note: Filter capacitors values are informative and application dependent, 0.1 μF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Recommended filtering is only valid for dedicated passive copper cable ports. For ports supporting both passive and active modules use recommended filtering from Figure 3 or 4.

Figure 5: Example QSFP-DD host board schematic of Passive Copper Cables Module

4.4 Low Speed Electrical Specification

TWI bus composed of the initiator and the target devices. The initiator controls the bus and the target device respond to the initiator requests.

4.4.1 TWI Logic Levels and Bus Loading

Low speed signaling other than the SCL and SDA interface is based on Low Voltage (LVTTL/LVCMOS) operating at Vcc. This specification is similar to SFF-8679 [35] for operation up 400 kHz but this specification also supports 1 MHz operation. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc host on each of the TWI interface SCL (clock), SDA (data), and all low speed status outputs (see Table 7). The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

The QSFP-DD/QSFP-DD800/QSFP-DD1600 low speed electrical specifications are given in Table 7, where some of the parameters are more stringent than JEDEC JESD8C [19]. Implementations compliant to this specification ensures compatibility between TWI host bus initiator and the TWI target device.

Table 7- Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL (max)=3 mA for Fast Mode, 20 mA for Fast Mode+
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	Capacitance of SCL and SDA in this specification are higher than [20] to account for connector and trace capacitances.
Total bus capacitive load for SCL and SDA	Cb		400	pF	Maximum bus capacitance for Fast-Mode (400 kHz), see [20]. For allowed range of bus capacitance and pullup resistors, see Figure 7 and Figure 8.
			550	pF	Maximum bus capacitance for Fast-Mode+ (1 MHz), see [20]. For allowed range of bus capacitance and pullup resistors, see Figure 7 and Figure 8.
LPMode/TxDis, ResetL, ModSelL and ePPS/Clock	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
P/VS[1, 2, 3, 4]	VIL		TBD	V	
P/VS[1, 2, 3, 4]	VIH		TBD		
LPMode, ResetL and ModSelL	|Iin|		360	µA	0V<Vin<Vcc
ePPS/Clock	|Iin|		6.5	mA	0V<Vin<Vcc
P/VS[1, 2, 3, 4]	|Iin|		TBD		
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0 mA
	VOH	Vcc-0.5	Vcc+0.3	V	10 kΩ pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0 mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

4.5 Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. The QSFP-DD/QSFP-DD800/QSFP-DD1600 memory map are based on “Common Management Interface Specification (CMIS)” [5]. Some timing requirements are critical, especially for a multi-lanes device, so the interface speed may optionally be increased. Byte 00h on the Lower Page or Address 128 Page 00h is used to indicate the use of the QSFP-DD/QSFP-DD800/QSFP-DD1600 memory map rather than the QSFP memory map. When a QSFP+ module is inserted into a QSFP-DD/QSFP-DD800 port the host must determine which memory map to use (e.g., SFF-8636 [33] or CMIS [5]) based on the QSFP+ identifier at Byte 00h on the Lower Page or Address 128 Page 00h. Operation of QSFP+ in QSFP-DD/QSFP-DD800/QSFP-DD1600 host is outside the scope of this document.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated. In cases where a status or control aspect is applicable only to lanes after muxing or demuxing has occurred, the status or control is intended to apply to all lanes in the mux group, unless otherwise indicated.

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc, [19]. Hosts shall use a pull-up resistor connected to Vcc_host on the TWI interface SCL (clock) and SDA (Data) signals. Detailed electrical specifications are given in 4.4. Timing specifications for management functionality involving electrical low speed signals are found are given in Table 9.

Nomenclature for all registers more than 1 bit long is MSB-LSB.

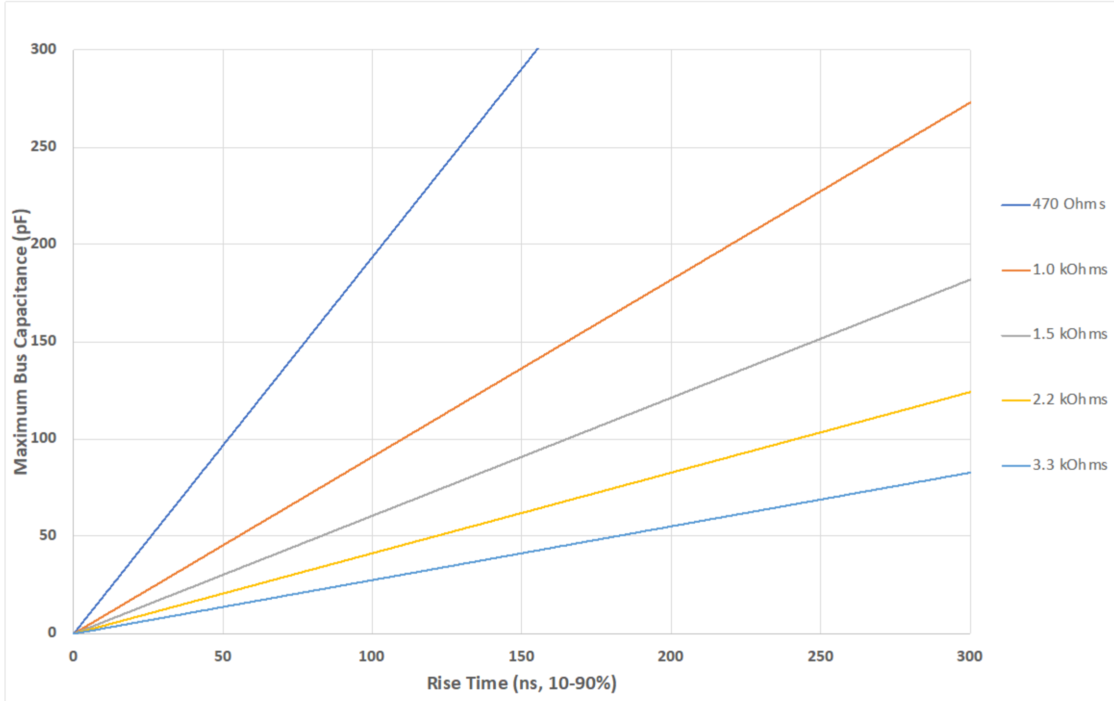
4.5.1 Management Interface Timing Specification

The timing parameters for the TWI interface (TWI) to the QSFP-DD/QSFP-DD800/QSFP-DD1600 module memory transaction timings are shown in Figure 6 and specified in Table 8 and is compatible with I2C [20]. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. The total bus capacitance in conjunction with the SCL/SDA pull resistor determines the speed TWI could operate, 4.5.2 provide pull up resistor for bus capacitance and speed. This clause closely follows the QSFP+ SFF-8636 [33] specification with the addition of Fast Mode+. This specification also defines tBUF timing, tWR timing, tNACK timing, tBPC timing.

Figure 6: TWI Timing Diagram

4.5.2 TWI Bus Pull Up Resistor

The maximum SCL/SDA pull resistors is based on the total bus capacitance, operating voltage, and the bus speed. Analysis is based on I2C specifications [20] with some exception, the ViH/ViH in QSFP-DD MSA are based on [0.75/0.25]*VCC instead of [0.7/0.3]*VCC as specified in the I2C specifications. QSFP-DD maximum bus capacitance and pull up resistor will be slightly lower than the I2C specifications. Figure 7 show maximum bus capacitance as function of rise time for several pull up resistors. Figure 8 show maximum pull up resistor Rp for Fast-mode and Fast-mode plus as function of total bus capacitance to meet the maximum rise time for Fast-mode and Fast-mode plus. In Figure 8 minimum Rp is limited to 1100 Ω due to Fast Mode driver capable of only sourcing (I_{OL}) ≤ 3 mA and the figure also doesn't show Rp for greater than 400 pF bus capacitance in case of Fast Mode+ with (I_{OL}) ≤ 20 mA due to excessive power dissipation (Fast-mode plus specifications allow up to 550 pF total bus capacitance [20]).



1
2 **Figure 7: Maximum Bus Capacitance for Several Pull Up Resistors**
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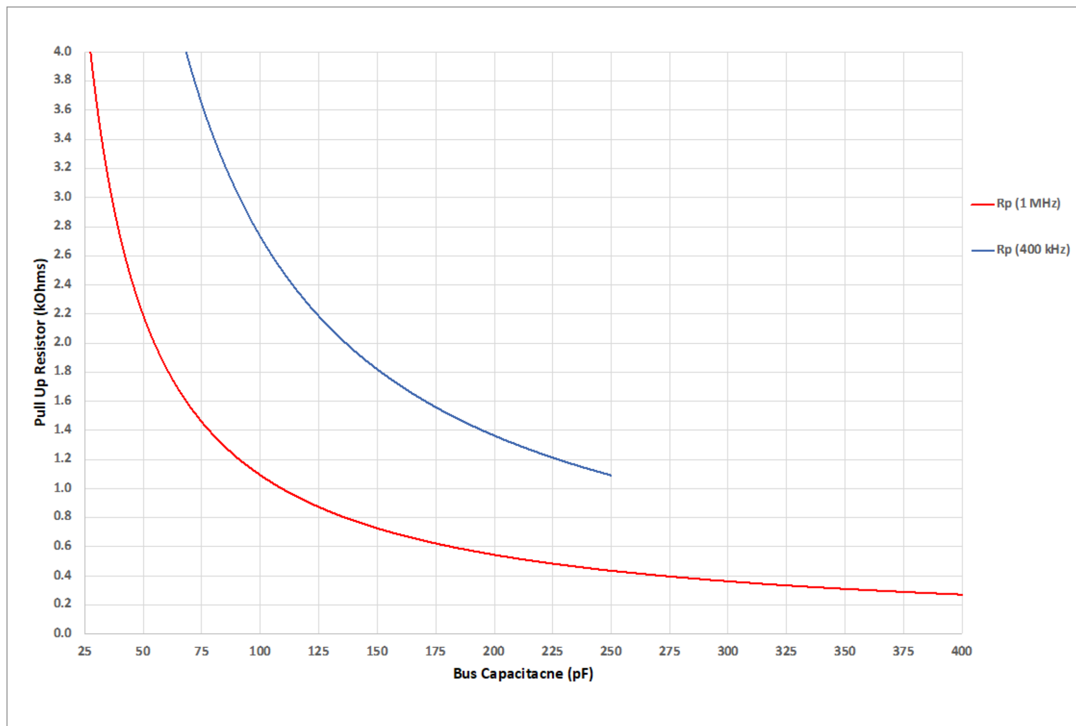

5
6 **Figure 8: TWI Pull Up Resistor as Function of Total Bus Capacitance**
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Table 8- Management Interface timing parameters

TWI Modes		Fast Mode (400 kHz)		Fast Mode+ (1 MHz)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	t_R		300		120	ns	Maximum pullup resistor Rp (assuming ViH/ViH [0.75/0.25]*VCC), see Figure 8
Input Fall Time	t_F		300		120	ns	
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Aborted sequence – bus release	Deselect _Abort		2		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time[1]	tSU. ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host-initiated TWI serial bus sequence.
ModSelL Hold Time[1]	tHD. ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a TWI serial bus sequence to changes of module select status.
TWI Serial Interface Clock Holdoff “Clock Stretching”	T_clock_ hold		500		500	µs	Time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non-volatile registers	tWR		80		80	ms	Time to complete a Single or Sequential Write to non-volatile registers.
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50k		50k		cycles	Module Case Temperature = 70 ºC
Note 1: CMIS management registers can be read to determine alternate ModSelL set up and hold times. See CMIS 8.4.5, Durations Advertising.							

1 The TWI serial interface address of the QSFP-DD module is 1010000X (A0h). In order to allow access to
2 multiple QSFP-DD/QSFP-DD800/QSFP-DD1600 modules on the same TWI serial bus, the QSFP-DD/QSFP-
3 DD800/QSFP-DD1600 includes a module select pad, ModSelL. This input (which is pulled high, deselected in
4 the module) must be held low by the host to select the module of interest and allow communication over the
5 TWI serial interface. The module must not respond to or accept TWI serial bus instructions unless it is
6 selected.
7
8 Before initiating a TWI serial bus communication, the host shall provide setup time on the ModSelL line of all
9 modules on the TWI bus. The host shall not change the ModSelL line of any module until the TWI serial bus
10 communication is complete and the hold time requirement is satisfied.
11

12 ### 4.5.3 Timing for soft control and status functions

13 Timing for QSFP-DD/QSFP-DD800/QSFP-DD1600 soft control status functions are described in Table 9.
14 Squelch and disable timings are defined in Table 10.
15

Table 9- Timing for QSFP-DD soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1], hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	10		μs	Minimum pulse time on the ResetL signal to initiate a module reset.
Int/RxLOS Mode Change	t_IntL/RxLOSL		100	ms	Time to change between IntL and RxLOSL modes of the dual- mode signal IntL/RxLOSL.
LPMode/TxDis mode change time	t_LPMode/TxDis		100	ms	Time to change between LPMode and TxDis modes of LPMode/TxDis.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
IntL Deassert Time	toff_IntL		500	μs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
RxLOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted [3].
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted [3].
RxLOS Deassert Time (optional fast mode)	toff_f_LOS		3	ms	Optional fast mode is advertised via the CMIS. Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.
TX Disable Assert Time	ton_TxDis		100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.
TX Disable Assert Time (optional fast mode)	ton_f_TxDis		3	ms	Optional fast mode is advertised via CMIS. Time from TxDis signal high to the optical output reaching the disabled level.
TX Disable Deassert Time	toff_TxDis		400	ms	Time from Tx Disable bit cleared to 1 until optical output rises above 90% of nominal [4].
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.

Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b) [5] until associated IntL assertion is inhibited.
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b) [5] until associated IntL operation resumes
Data Path Tx Turn On Max Duration[6]	DataPathTxTurnOn_MaxDuration				see CMIS memory P01h: B168
Data Path Tx Turn Off Max Duration[6]	DataPathTxTurnOff_MaxDuration				see CMIS memory P01h: B168
Data Path Deinit Max Duration[6]	DataPathDeinit_MaxDuration				see CMIS memory P01h: B144
Data Path Init Max Duration[6]	DataPathInit_MaxDuration				see CMIS memory P01h: B144
Module Pwr Up Max Duration[7]	ModulePwrUp_MaxDuration				see CMIS memory P01h: B167
Module Pwr Dn Max Duration[7]	ModulePwrDn_MaxDuration				see CMIS memory P01h: B167

Notes: 1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 13.
2. Measured from low to high SDA edge of the Stop condition of the read transaction.
3. Rx LOS condition is defined at the optical input by the relevant standard.
4. Tx Squelch Deassert time is longer than SFF-8679 [35].
5. Measured from low to high SDA edge of the Stop condition of the write transaction.
6. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol, unless the module advertises a less than 1 ms duration in which case there is no defined measurement.
7. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol.

1

Table 10- I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached, see 4.6.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached, see 4.6.2.
Tx Squelch Deassert Time	toff_Txsq	1.5	s	Tx squelch deassert is system and implementation dependent, see also 4.6.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence[1] until optical output falls below 10% of nominal.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal, see notes 2 and 3.
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see notes 2, and 3.
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see notes 2 and 3.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.
Notes: 1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction. 2. CMIS 4.0 and beyond the listed values are superseded by the advertised DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in P01h.168. 3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times (P01h.168) that can be advertised by such modules (for CMIS 4.0 and beyond).				

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4.6 High Speed Electrical Specification

For detailed QSFP-DD electrical specifications for operation up to 29 GBd see e.g., IEEE Std 802.3-2018 Annex 86A, Annex 83E, Annex 120C, or Annex 120E [14]; Fibre Channel FC-PI-6 [1], FC-PI-7 [2]; OIF CEI 4.0 [21]; InfiniBand FDR, EDR, and HDR specifications [18]. For detailed QSFP-DD-800 electrical specifications for operation up to 56 GBd see e.g., IEEE P802.3ck Annex 120G [15]; Fibre Channel FC-PI-8 [3]; OIF CEI-112G-VSR [21]; InfiniBand NDR specifications [18].

Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations of the following subsections 4.6.1 and 4.6.2 may be used.

4.6.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP-DD/QSFP-DD800/QSFP-DD1600 module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP-DD/QSFP-DD800/QSFP-DD1600 modules and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or as defined by the relevant standard, or whichever is less.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output lane(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output lane as shown in Table 15. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the TWI serial interface. Rx Squelch Disable is an optional function.

4.6.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP-DD module transmitter data inputs. They are AC-coupled 100 Ω differential lines with 100 Ohm differential terminations inside the QSFP-DD/QSFP-DD800/QSFP-DD1600 optical module. The AC coupling is implemented inside the QSFP-DD optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input lane becoming less than the TX Squelch Levels specified in Table 11 when terminated in to 100 Ω differential, then the transmitter optical output associated with that electrical input lane shall be squelched and the associated TxLOS flag set. If multiple electrical input lanes are associated with the same optical output lane, the loss of any of the incoming electrical input lanes causes the optical output lane to be squelched.

Table 11- TX Squelch Levels

Data Rate	Levels	Unit
OIF 28G-VSR/IEEE CL83E	70	mV [1]
OIF 56G-VSR/IEEE CL120E	70	mV [1]
OIF 112G-VSR/IEEE CL120G	50	mV [1]
1. Differential peak-peak.		

For applications, e.g., Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g., InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the TWI serial interface. Tx Squelch and Tx Squelch Disable are optional functions.

4.7 Power Requirements

The QSFP-DD module paddle card power supply has six designated pads, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination at the discretion of the module vendor, see note 2 in Table 1. Power is applied concurrently to these pads.

A host board together with the QSFP-DD/QSFP-DD800/QSFP-DD1600 module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion or module state transitions.

All power supply requirements in Table 13 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.7.1 Power Classes and Maximum Power Consumption

There are two power modes: Low Power Mode and High Power Mode, and eight power classes, Class 1 - Class 8. Module power classes are defined in Table 12 and module power specifications are provided in Table 13.

Since a wide range of module power classes exists, to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to accommodate only low power consumption modules, it is recommended that host systems designed to accommodate only low power consumption modules also implement the state machine defined in the CMIS [5] and identify the power class of the module before allowing the module to go into High Power Mode, where power class 8 requires reading CMIS (Page00, Byte 201) to determine actual power consumption. This is to avoid exceeding the host system power supply limits and cooling capacity when a module exceeding the power class supported by the system is inserted.

Table 12- Power Classes

Power Class	Max Power (W)	CMIS Register
1	1.5	Direct readout of Page 00h Byte 200[000xxxxx]
2	3.5	Direct readout of Page 00h Byte 200[001xxxxx]
3	7.0	Direct readout of Page 00h Byte 200[010xxxxx]
4	8.0	Direct readout of Page 00h Byte 200[011xxxxx]
5	10	Direct readout of Page 00h Byte 200[100xxxxx]
6	12	Direct readout of Page 00h Byte 200[101xxxxx]
7	14	Direct readout of Page 00h Byte 200[110xxxxx]
8 [1]	>14	Direct readout of Page 00h Byte 200[111xxxxx]
Note: 1. When a module reports power class 8 the host must read CMIS Page 00h Byte 201 to determine module power dissipation. Please see CMIS Byte 201 register definition for more information.		

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements. Utilization of the maximum QSFP-DD power rating requires thermal design and

validation at the system level to ensure the maximum connector temperature is not exceeded, see A.2. A recommended design practice for host supporting power class 8 (>~20 W) is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

4.7.2 Host Board Power Supply Filtering

The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of module Power Classes. During power transient events, the host should ensure that any neighboring modules sharing the same supply stay within their specified supply voltage limits. The host should also ensure that the intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules. An example reference power supply filter is shown in Figure 9.

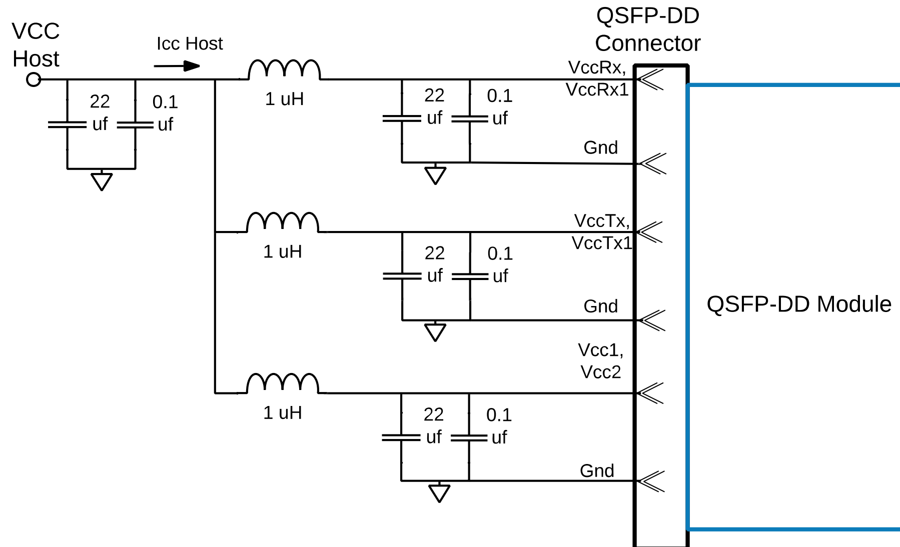


Figure 9: Reference Power Supply Filter for Module Testing

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. System designers should choose components with appropriate DCR and ESR, to minimize the voltage drop and the amount of noise coupled to the module. Hosts supporting higher power classes modules may require additional design considerations, in order to minimize the voltage drop and the amount of noise coupled to the module.

The specifications for the power supply are shown in Table 13. The limits in Table 13 apply to the combined current that flows through all inductors in the power supply filter (represents host Icc current in Figure 9). Inrush current shall be measured with the appropriate equipment, such as current probes or shunt resistors. The test equipment shall provide enough bandwidth, vertical resolution, SNR and memory depth, in order to capture properly all the power events.

4.7.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, if the host pulls LPMode high, upon hot-plug, power cycle or reset, QSFP-DD/QSFP-DD800/QSFP-DD1600 modules shall power up in Low Power Mode. If the host pulls LPMode low, the module will proceed to High Power Mode without host management intervention. Figure 10 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power classes are given in Table 13. Host output noise limit, module output noise limit, and module input noise tolerance limit are given in Table 14.

The module shall not be affected by the instantaneous variations of the power supply caused by its own current drawing profile during all power transient events. The module shall support instantaneous power supply Vcc variations with a slew rate up to 175 mV/ms. No traffic hits or TWI errors shall be observed during Vcc variations.

Table 13- Power supply specifications, instantaneous, sustained, and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1, Vcc1 & Vcc2 including ripple, droop and noise below 100 kHz[1]		3.135	3.3	3.465	V
Module inrush - instantaneous peak duration[2]	T_ip			50	µs
Module inrush - initialization time[2]	T_init			500	ms
Low Power Mode for all modules and Power Class 1 module					
Power Consumption Class	P_0			1.5	W
Instantaneous peak current at hot plug	Icc_ip_lp	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_lp	-	-	495	mA
Steady state current	Icc_lp	See Note 3			mA
High Power Mode Power Class 2 module					
Power Consumption Class	P_2			3.5	W
Instantaneous peak current	Icc_ip_2	-	-	1400	mA
Sustained peak current	Icc_sp_2	-	-	1155	mA
Steady state current	Icc_2	See Note 3			mA
High Power Mode Power Class 3 module					
Power Consumption Class	P_3			7	W
Instantaneous peak current	Icc_ip_3	-	-	2800	mA
Sustained peak current	Icc_sp_3	-	-	2310	mA
Steady state current	Icc_3	See Note 3			mA
High Power Mode Power Class 4 module					
Power Consumption Class	P_4			8	W
Instantaneous peak current	Icc_ip_4	-	-	3200	mA
Sustained peak current	Icc_sp_4	-	-	2640	mA
Steady state current	Icc_4	See Note 3			mA
High Power Mode Power Class 5 module					
Power Consumption Class	P_5			10	W
Instantaneous peak current	Icc_ip_5	-	-	4000	mA
Sustained peak current	Icc_sp_5	-	-	3300	mA
Steady state current	Icc_5	See Note 3			mA
High Power Mode Power Class 6 module					
Power Consumption Class	P_6			12	W
Instantaneous peak current	Icc_ip_6	-	-	4800	mA
Sustained peak current	Icc_sp_6	-	-	3960	mA
Steady state current	Icc_6	See Note 3			mA
High Power Mode Power Class 7 module					
Power Consumption Class	P_7			14	W
Instantaneous peak current	Icc_ip_7	-	-	5600	mA
Sustained peak current	Icc_sp_7	-	-	4620	mA
Steady state current	Icc_7	See Note 3			mA
High Power Mode Power Class 8 module					
Power Consumption Class	P_8[4]			>14	W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	12	A

Notes: 1. Measured at VccTx, VccTx1, VccRx, VccRx1, Vcc1 and Vcc2.
2: T_ip and T_init are test conditions for measuring inrush current and not characteristics of the module
3: The module must stay within its declared power class.
4: P_8 is the module power dissipation reported by CMIS Byte 201.

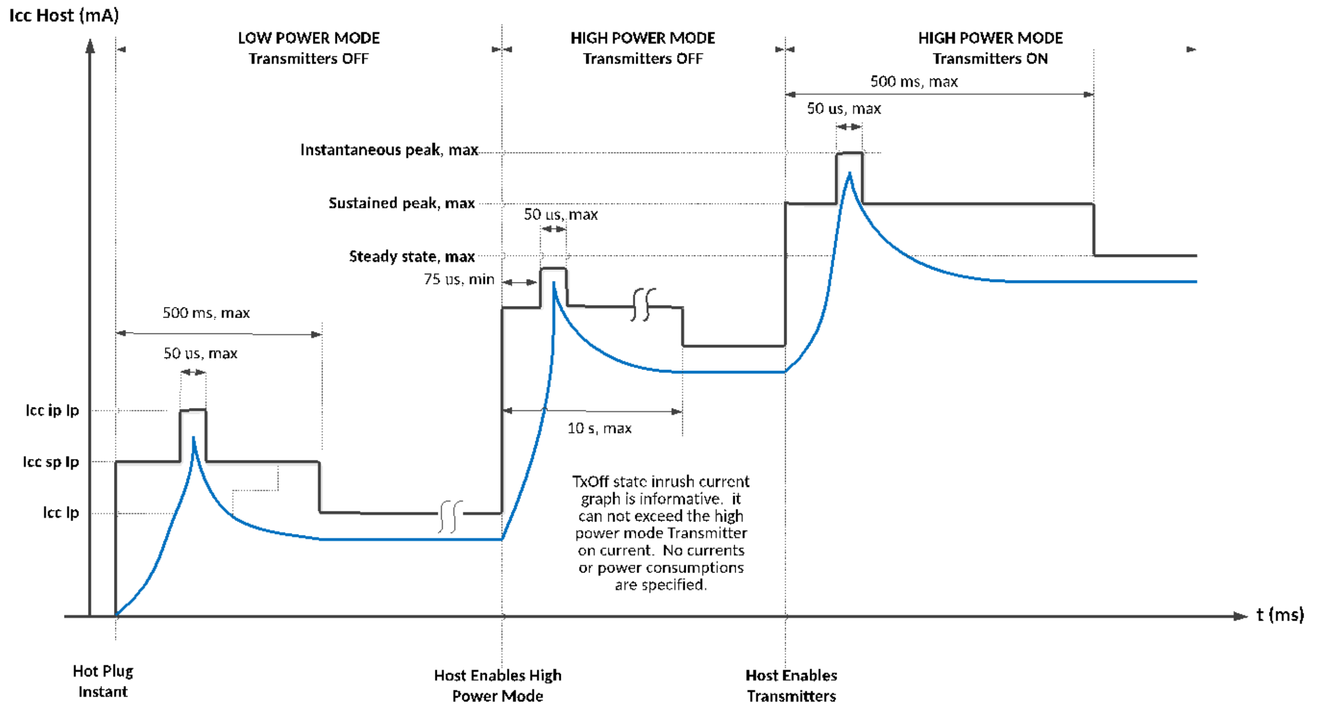


Figure 10: Instantaneous and sustained peak currents for Icc Host (see Table 13)

Table 14- Host and Module Output Noise and Tolerance Specifications

Parameter	Symbol	Min	Nom	Max	Unit
Host RMS noise output 40 Hz-10 MHz (eN_Host)[1]				25	mV
Module RMS noise output 40 Hz - 10 MHz [2]				150	mA
Module sinusoidal power supply noise tolerance 40 Hz - 10 MHz (p-p) [2, 3]	$PSNR_{mod}$			66	mV

1. Host must be tested for all supported power classes.
2. Module must be tested at low and high power modes.
3. Recommended test frequency sweep:
   40, 50, 60, 70, 80, 90 Hz
   100, 200, 300, 400, 500, 600, 700, 800, 900 Hz
   1, 2, 3, 4, 5, 6, 7, 8, 9 kHz
   10, 20, 30, 40, 50, 60, 70, 80, 90 kHz
   100, 200, 300, 400, 500, 600, 700, 800, 900 kHz
   1, 2, 3, 4, 5, 6, 7, 8, 9, 10 MHz.

4.7.4 Host Board Power Supply Noise Output

The host noise output on Vcc1/Vcc2, VccTx/VccTx1, and VccRx/VccRx1 supplies are defined with resistive loads that draws the maximum rated power supported by the host power class, see Figure 11. The resistive loads are connected in place of the module between Vcc1/Vcc2, VccTx/VccTx1, and VccRx/VccRx1 and the Vee. When the noise is measured on the three voltage rails Vcc1/Vcc2, VccTx/VccTx1, and VccRx/VccRx1, the noise is measured independently on each rail, and the two voltage rails not being tested are left open circuit. Host power supply limits are given in Table 12. The noise power spectrum is measured for each of the

3 rails then integrated from 40 Hz to 10 MHz and converted to a voltage, eN_Host, with limit specified Table 14.

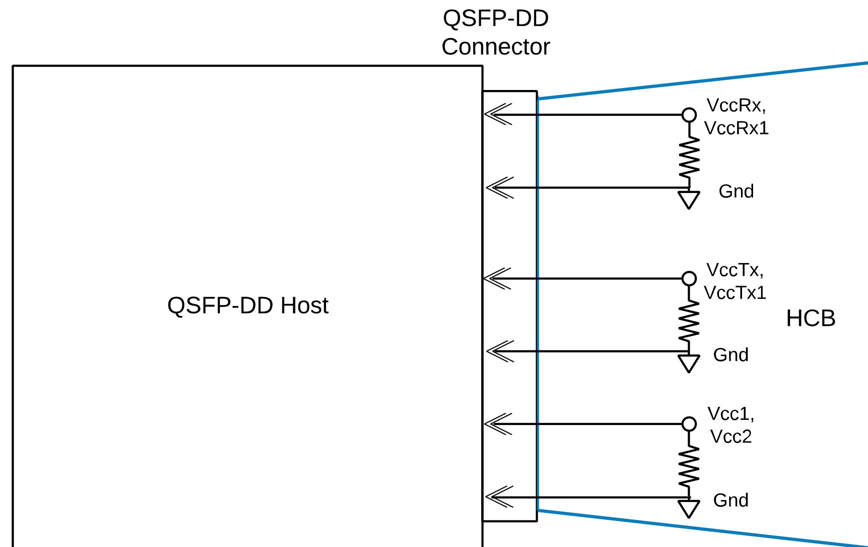


Figure 11: Host Noise Output Measuremnt

4.7.5 Module Power Supply Noise Output

The QSFP-DD/QSFP-DD800/QSFP-DD1600 modules, when plugged into a reference module compliance board, shall generate noise current less than the value in Table 14. The module must pass module power supply noise output current test in all operating modes. This test ensures the module will not couple excessive noise from in- side the module back onto the host board. This improved test method no longer uses series resistor as introduced in the SFF-8431 and instead for improved accuracy uses a current probe with a scope capable of integrating the current noise from 40 Hz to 10 MHz.

Rogowski probes are recommended because they will minimize added interconnect inductance, example of such probes are Tektronix TRCP series, Keysight N7042A or similar. Hall-effect current probes may also be acceptable if added interconnect is negligible, example of such probes are Tektronix TCP, Keysight N1147B.

The RMS module noise current output is defined in the frequency band from 40 Hz to 10 MHz. Module noise current output shall be measured with a current probe at point X, see Figure 12 and must meet limits given in Table 14. The leads from point X to the system power supply must be kept as short as possible to minimize the impact of added lead inductance. The module must pass module power supply noise output test in all operating modes. This test ensures the module will not couple excessive noise from inside the module back onto the host board.

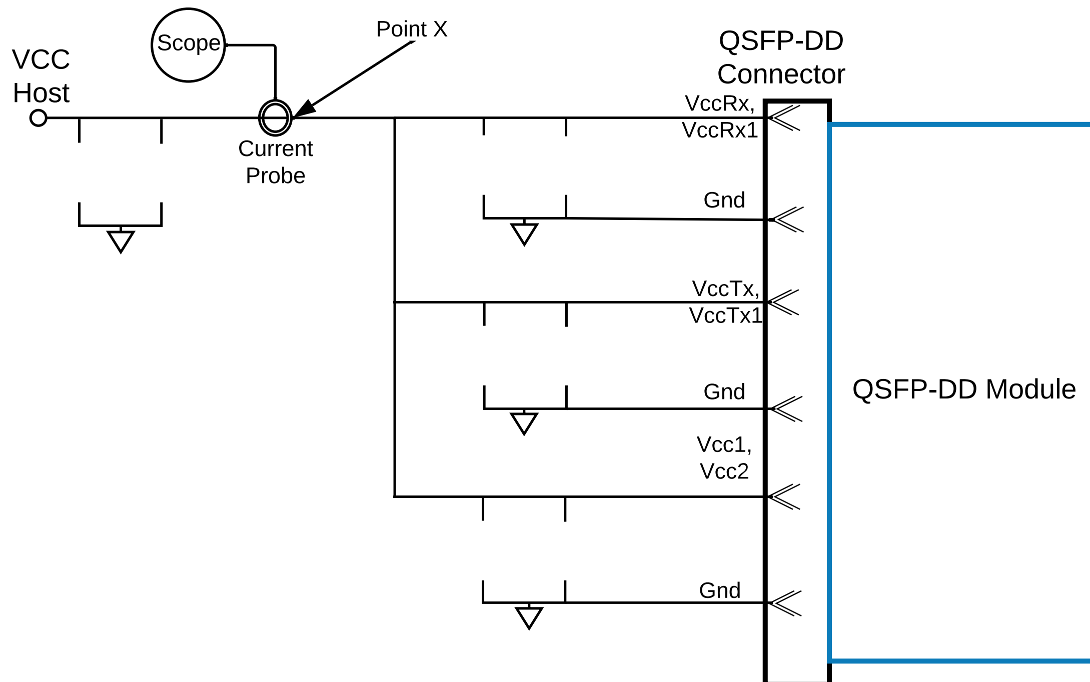


Figure 12: Module Noise Output Measurement

4.7.6 Module Power Supply Noise Tolerance Methods

4.7.6.1 Module Power Supply Noise Tolerance with OpAmp

The QSFP-DD/QSFP-DD800/QSFP-DD1600 modules shall meet all requirements and operate within the design specifications in the presence of a reference noise waveform described in Table 14 superimposed on the DC voltage. The reference noise waveform consists of a sinusoidal 40 Hz to 10 MHz noise generated by Osc1 and added to Vcc PSU, see Figure 13. This emulates the worst-case noise that the module must tolerate while meeting or exceeding the design specifications. The reference noise is generated by Osc1 and amplified by the Power OpAmp then added to Vcc PSU through a Bias-T, see Figure 13. Example of suitable Power OpAmp are Analog Devices ADA4870, LT1210, TI THS3491. Since most of these power OpAmps are limited to 1Amp peak, the interconnecting impedance of the Bias-T must be greater than 33mVpk/1Apk or 33 mΩ minimum. Based on the minimum suggested frequency of 100 kHz, this can be resistive (33 mΩ) or reactive (47nH) minimum. The Bias T effective capacitor needs to be greater than 47 µF, so a stable tantalum capacitor with 30 mΩ ESR is recommended. With power supply filter components removed, point X measures the noise voltage applied to the module. To facilitate power supply tolerance testing at frequencies < ~100 kHz due to Power OpAmp interaction with PSU and low frequency response of the Bias-T, it is recommended to use noise source Osc2 modulating PSU sense line to generate sinusoidal noise directly on the PSU output, see Figure 14. Osc2 amplitude level is adjusted while observing point X amplitude level as defined in Table 14 for module in low power and high-power modes. To modulate the PSU sense lines, the PSU must have high speed sense tracking. An example of PSU with high-speed sense tracking are Keysight N6700 Series, Kikusui PBZ series, or supply controllers, such as the TI TPSM5D1806.

The user is responsible for the calibration and the validation of the setup across the whole frequency range. The user may need to consider alternative proposed solutions if the electrical characteristics of the fixture setup requires any component to work beyond the safety operating conditions.

For modules without or with limited input stage power filtering the applied noise to the module may be measured at point X directly while the module is active and either in low or high-power modes. To compensate for input stage power filtering in the module, the module under test is replaced with a resistive load drawing

equivalent current of a module configured in low power mode, the module under test is then replaced with a resistive load drawing equivalent current of a module configured in high power mode. Osc1 and Osc2 are adjusted to produce maximum PSNR level as defined in Table 14 at point X with resistive loads drawing the same power as the module in low and high-power modes. The resistive loads are then replaced with the module under test, with the same Osc1/Osc2 amplitude settings that produced the max PSNR with the resistive loads.

Notes: An appropriate probing technique (such as transmission line probe) is required for noise measurement at point X, [30] [31]. For modules with limited or no decoupling directly connected to host PSU, the PSNR can be directly measured at point X with the module plugged into the host and the module operating in low power and high power modes. Osc1 or Osc2 are adjusted to provide maximum PSNR at point X for a given module in low power and full power modes. Depending on the measurement setup, a ground loop isolator may be required, see [30] and [31].

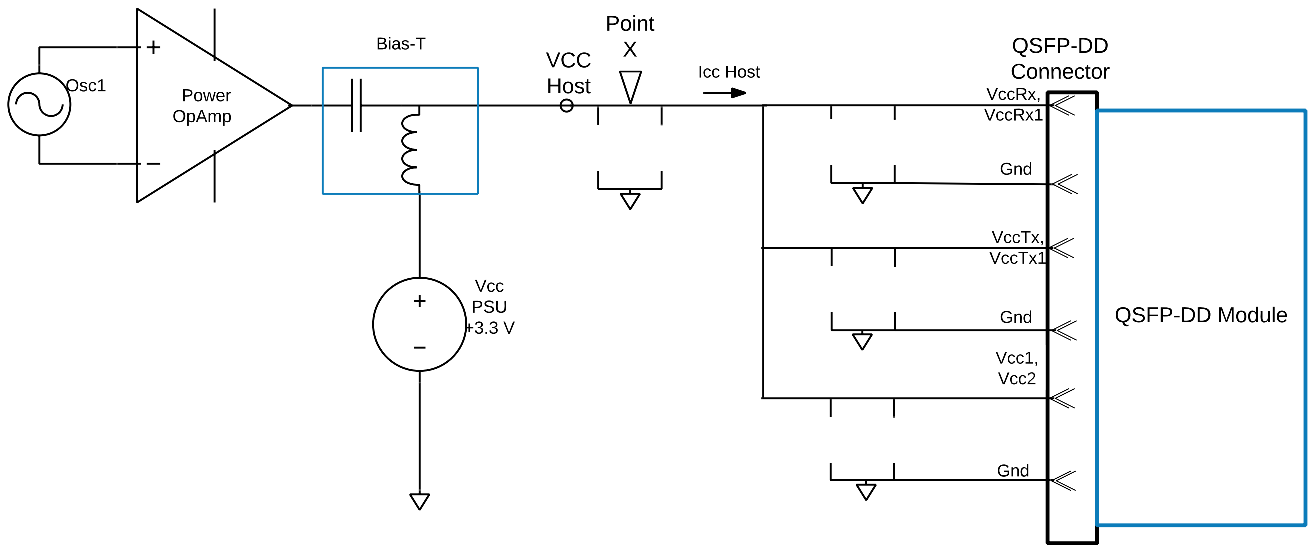


Figure 13: Module High Frequency Noise Tolerance

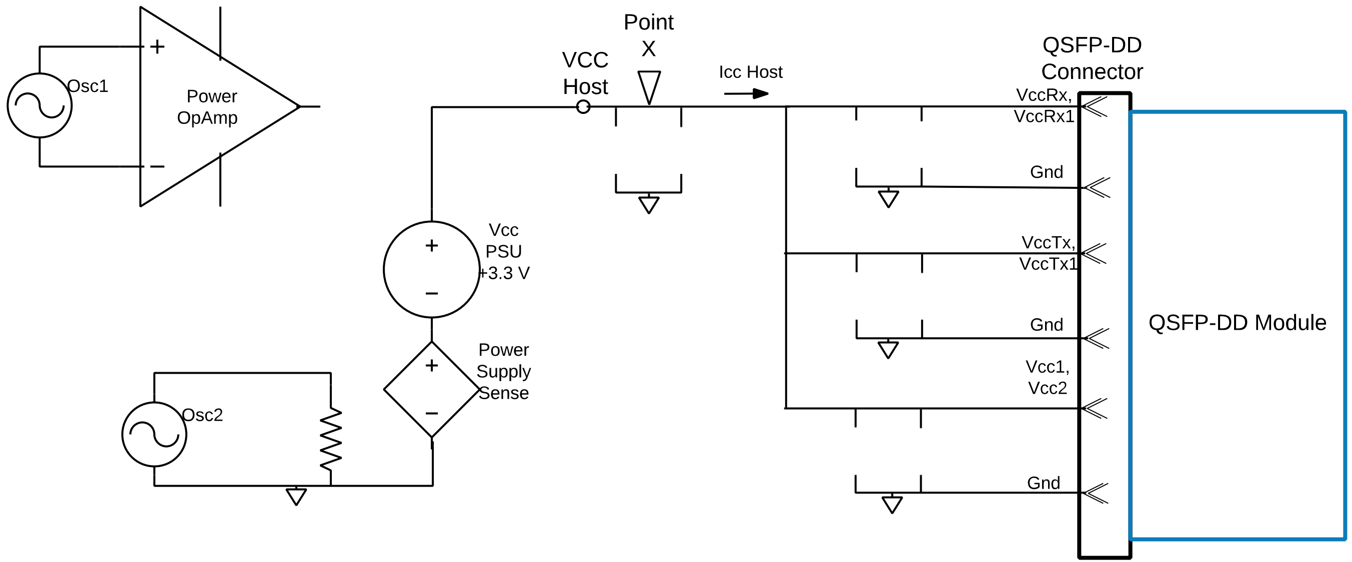
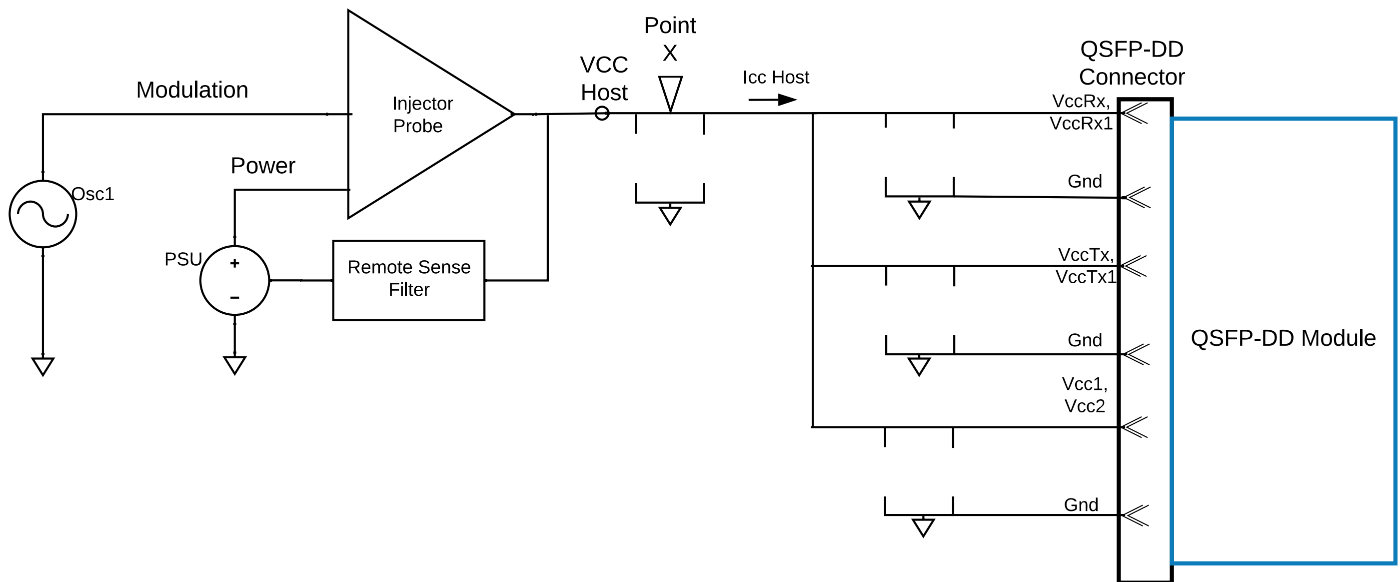


Figure 14: Module Low Frequency Noise Tolerance

4.7.6.2 Module Power Supply Noise Tolerance with Commercial Injector Probe

Module Power Supply Noise Tolerance implementation of 4.7.6 can be replaced with commercially produced injector probes, an example of such injector probe is Picotest P2124A, [29]. Injector probe combines a power rail voltage (input voltage) with a modulation signal and injects the noisy bus voltage into the module being tested for noise immunity (PSNR). The form factor of injector probe is such that it can be positioned at the card edge, eliminating power cables and the inductance that can limit the modulation amplitude and bandwidth. This modulation scheme supports the full 40 Hz-10 MHz range without having to change setups at ~100 kHz.

The probe-based implementation supports the requirements by getting close enough to the module under test to allow modulating up to 10 MHz with little attenuation. The DC input power supply voltage at the host can be held constant using a supplied remote sense filter. The remote sense filter allows the user to switch between different operating modes (high power, low power etc.) while keeping the operating point stable across every power state transition. With the appropriate PSU unit and remote filtering, the injector probe will compensate for any additional voltage drop due to the modulator and the interconnects.



1
2 **Figure 15: Broadband Noise Tolerance Injection Probe Setup**
3
4 **Injection Probe Setup Guideline, see [30] [31]**
5 • Injection probe may have sense line for optional remote sense.
6 • The modulated RF signal can be any 50 Ω generator.
7 • Usage of a remote sense filter to adjust the power supply voltage level is recommended.
8 • Benchtop power supply with greater than 3.6 V output range with sufficient current capabilities and with
9 sense line.
10
11

4.8 ESD

Where ESD performance is not otherwise specified, e.g., in the Ethernet specification, the QSFP-DD/QSFP-DD800/QSFP-DD1600 modules shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case. All the QSFP-DD/QSFP-DD800/QSFP-DD1600 modules and host pads including high speed signal pads shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JS-001 [8][19] and IEC EN61000-4-2 [7].

4.9 Clocking Considerations

4.9.1 Data Path Description

Within a module, host electrical and module media lanes are grouped together into a logical concept called a data path. A data path is intended to represent a group of lanes over which a block of data is distributed that will be powered up or down and initialized together. Some examples include a 100GAUI-4 to 100GBASE-SR4 module implementation, where the data path would include four host electrical lanes and four module media lanes, or a 400GAUI-8 to 400GBASE-DR4 module implementation, where the data path would include eight host electrical lanes and four module media lanes.

4.9.2 TX Clocking Considerations

Within a given Tx data path the host is responsible for ensuring that all electrical lanes delivered to the module are frequency synchronous (sourced from the same clock domain). If a module supports multiple Tx data paths running concurrently, the different Tx data paths can either all be in a single clock domain or separate clock domains. The module advertises which of these two modes it supports via the management registers.

If the module supports multiple Tx data paths running concurrently in a single clock domain, the module shall ensure that active Tx data paths continue to operate undisturbed even as other Tx data paths (and their associated Tx input lanes) are enabled/disabled by the host.

4.9.3 Rx Clocking Considerations

Within a given Rx data path all lanes received on the module media interface are required to be frequency synchronous (sourced from the same clock domain). If a module supports multiple Rx data paths running concurrently, the module shall allow the different Rx data paths to be asynchronous from each other (sourced from separate clock domains).

5 Optical Port Mapping and Optical Interfaces

5.1 Electrical data input/output to optical port mapping

Table 15 defines the mapping for QSFP-DD/QSFP-DD800/QSFP-DD1600 electrical Tx data inputs and Rx data outputs to optical ports combinations. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications. The QSFP+ 4 transmit lanes are [Tx1-Tx4] and 4 receive lanes are [Rx1-Rx4] allows optical port mapping as shown in Table 15, but the Tx/Rx lanes 5-8 should be ignored.

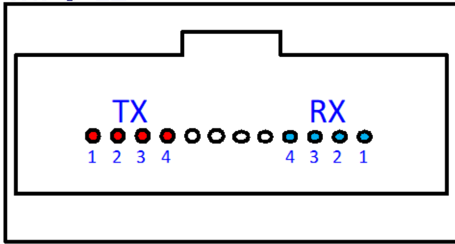
Table 15- Electrical Signal to Optical Port Mapping

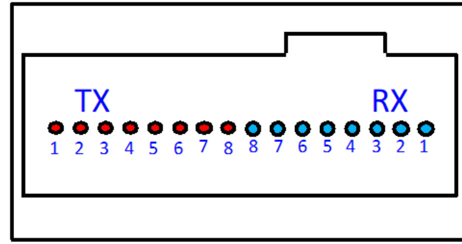
<table>
<tr><td rowspan="3">Electrical data input/output</td><td colspan="5">Optical port mapping (see Figure 16)</td></tr>
<tr><td>Duplex LC, CS, SN, or MDC</td><td>MPO-12, Dual (CS, SN, MDC, Duplex LC, or MPO-12)</td><td>MPO-12, Quad (SN or MDC)</td><td>MPO-12 (two row), MPO-16, or Dual MPO-12</td><td>MPO-12, SN, MDC (BiDi)</td></tr>
<tr><td>1 TX fiber
1 RX fiber [1]</td><td>2 TX fibers
2 RX fibers [1]</td><td>4 TX fibers
4 RX fibers [1]</td><td>8 TX fibers
8 RX fibers [1,3]</td><td>8 Tx (Rx) fibers [2,3]</td></tr>
<tr><td>Tx1</td><td rowspan="8">TX-1</td><td rowspan="4">TX-1</td><td rowspan="2">TX-1</td><td>TX-1</td><td>TR1</td></tr>
<tr><td>Tx2</td><td>TX-2</td><td>RT1</td></tr>
<tr><td>Tx3</td><td rowspan="2">TX-2</td><td>TX-3</td><td>TR2</td></tr>
<tr><td>Tx4</td><td>TX-4</td><td>RT2</td></tr>
<tr><td>Tx5</td><td rowspan="4">TX-2</td><td rowspan="2">TX-3</td><td>TX-5</td><td>TR3</td></tr>
<tr><td>Tx6</td><td>TX-6</td><td>RT3</td></tr>
<tr><td>Tx7</td><td rowspan="2">TX-4</td><td>TX-7</td><td>TR4</td></tr>
<tr><td>Tx8</td><td>TX-8</td><td>RT4</td></tr>
<tr><td>Rx1</td><td rowspan="8">RX-1</td><td rowspan="4">RX-1</td><td rowspan="2">RX-1</td><td>RX-1</td><td>RT1</td></tr>
<tr><td>Rx2</td><td>RX-2</td><td>TR1</td></tr>
<tr><td>Rx3</td><td rowspan="2">RX-2</td><td>RX-3</td><td>RT2</td></tr>
<tr><td>Rx4</td><td>RX-4</td><td>TR2</td></tr>
<tr><td>Rx5</td><td rowspan="4">RX-2</td><td rowspan="2">RX-3</td><td>RX-5</td><td>RT3</td></tr>
<tr><td>Rx6</td><td>RX-6</td><td>TR3</td></tr>
<tr><td>Rx7</td><td rowspan="2">RX-4</td><td>RX-7</td><td>RT4</td></tr>
<tr><td>Rx8</td><td>RX-8</td><td>TR4</td></tr>
<tr><td colspan="6">Notes:
1. TX-n or RX-n where n is the optical port number as defined Figure 16.
2. TRn or RTn where n is the optical port number as defined Figure 16.
3. Some QSFP-DD/QSFP-DD800/QSFP-DD1600 modules may require fewer CS, SN, or MDC connectors. In such cases, Port #1 is always the left-most port. Successive ports then follow sequentially from left-to-right as shown in Figure 16.</td></tr>
</table>

5.2 Optical Interfaces

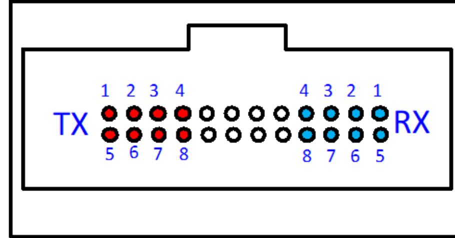
The recommended location and numbering of the optical ports for 14 Media Dependent Interfaces (MDI) are shown in Figure 16. The transmit and receive optical lanes shall occupy the positions depicted in Figure 16 when looking into the MDI receptacle with the connector keyway feature on top. QSFP-DD/QSFP-DD800/QSFP-DD1600 optical MDI examples are shown for three male MPO receptacles (see Figure 17, Figure 18, and Figure 19) a duplex LC (see Figure 20), a Dual CS connector (see Figure 21), a Quad SN receptacle (see Figure 22), a Quad MDC receptacle (see Figure 23), a Dual SN receptacle (see Figure 24),

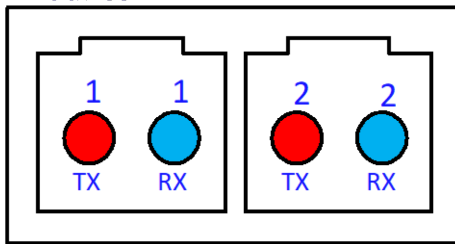
and a Dual MDC receptacle (see Figure 25), a Dual Duplex LC receptacle (see Figure 26), and a Dual MPO-12 receptacle (see Figure 29).

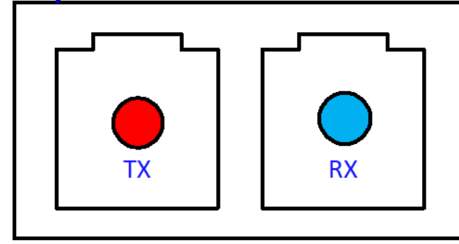


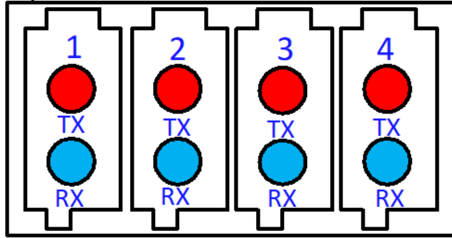


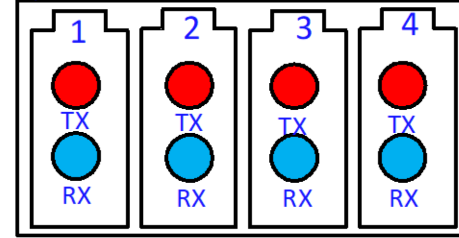
Note: The MPO 12, 2 row optical MDI is used for breakout applications and is not intended for structured cabling applications.

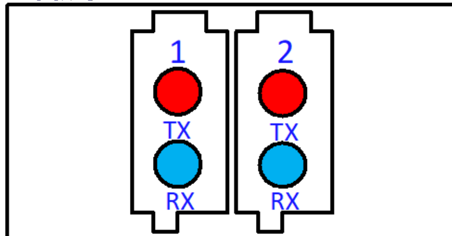


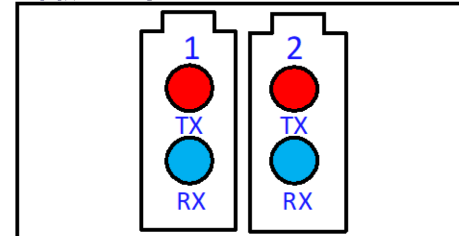


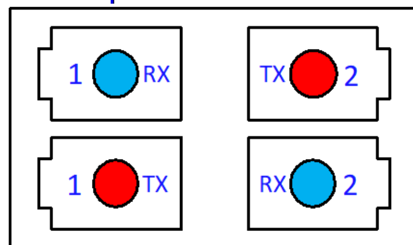


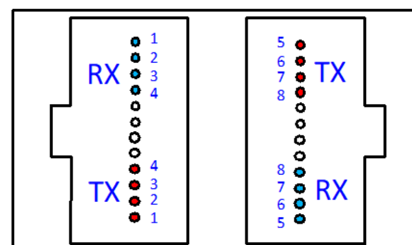




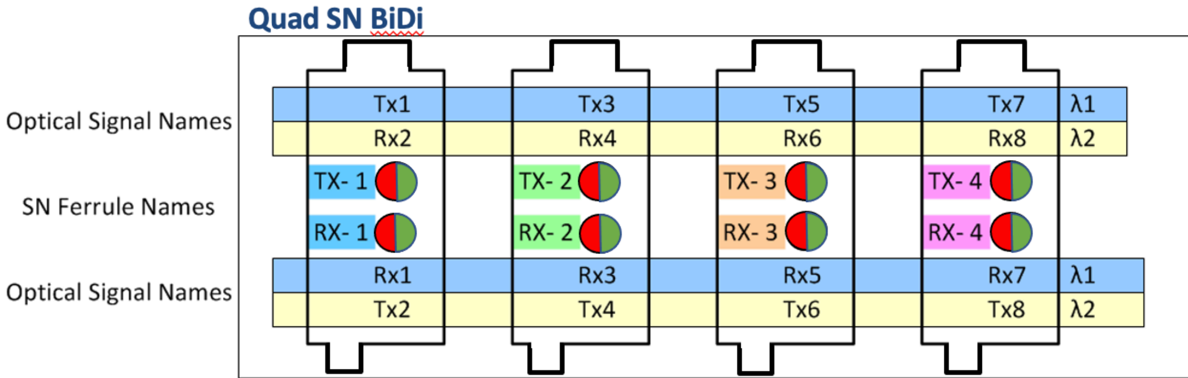


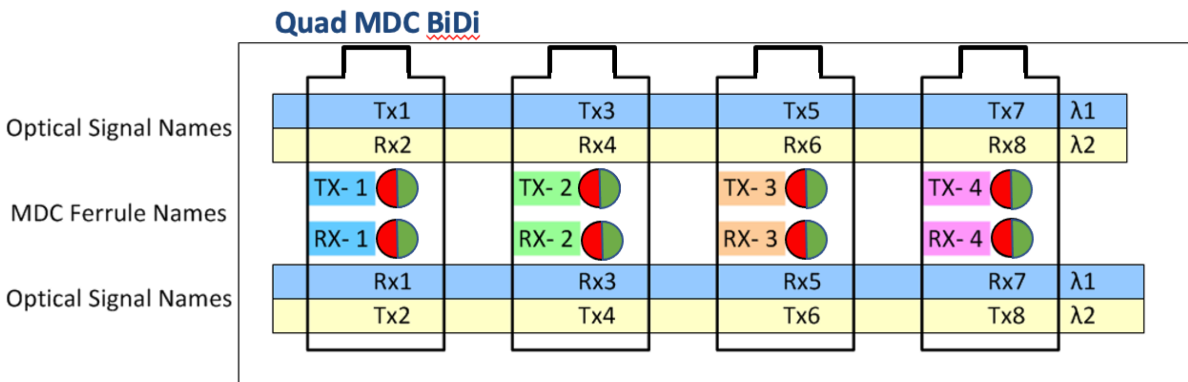




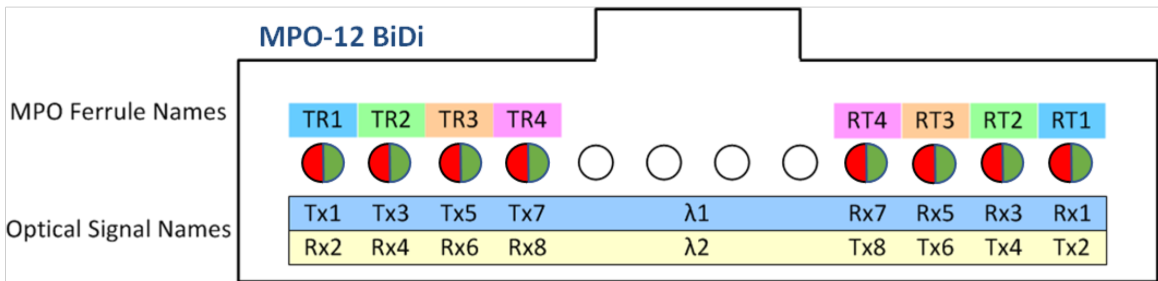


1





2
3
4

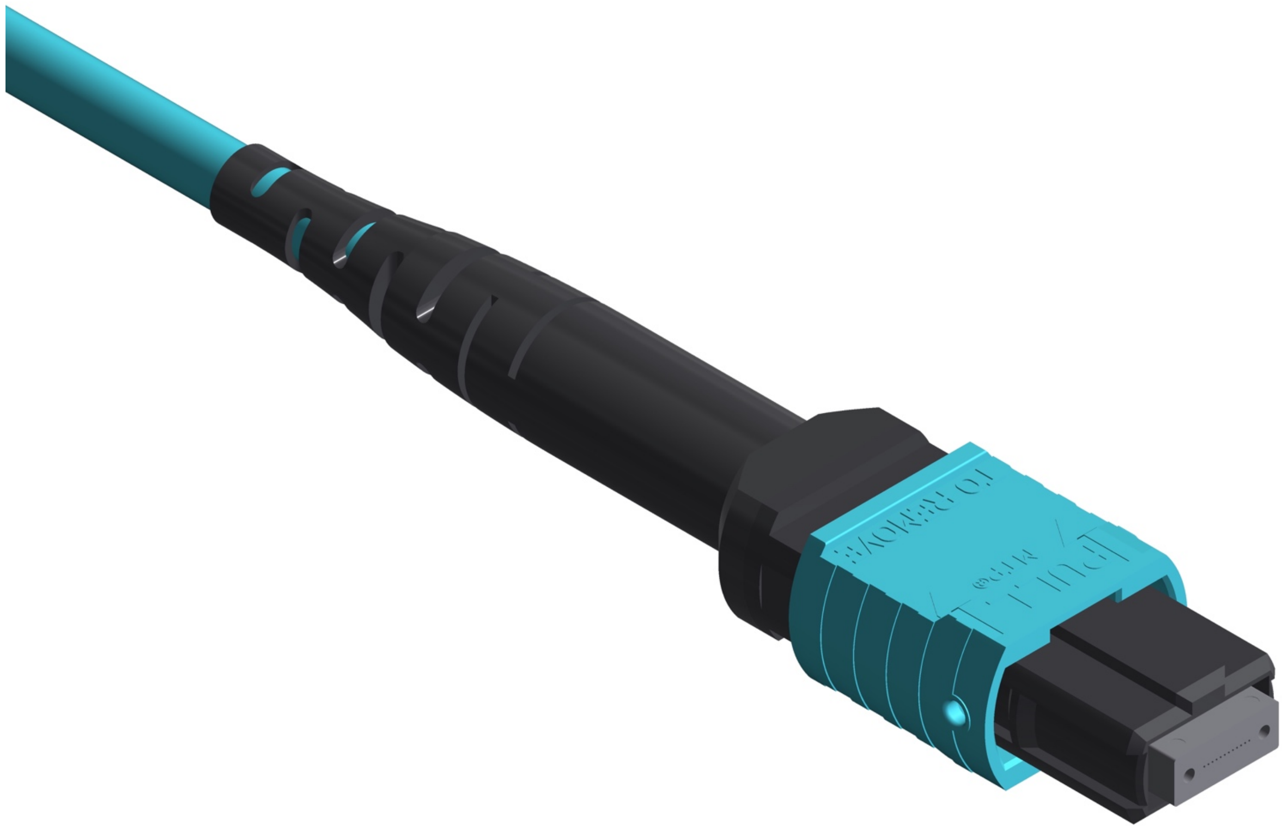


5
6
7 Note: For some CS, SN, and MDC use cases, fewer connector ports may be needed. In these cases, Port 1 is
8 always the left-most port. Successive ports then follow sequentially from left-to-right as shown. Dual Duplex
9 LC and Dual MPO port shall be positioned belly to belly, and the optical connector keys shall be oriented
10 towards the side walls of module.
11
12 **Figure 16: Optical Media Dependent Interface port assignments**
13

5.2.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 one row connectors are specified in TIA-604-5 [24] and IEC 61754-7-1 [10], see Figure 17. The optical plug and receptacle for one row MPO-16 connectors are specified in TIA-604-18 [26] and IEC 61754-7-3 [12] and shown in Figure 18. The optical plug and receptacle for the MPO-24 two row connectors are specified in TIA-604-5 [24] and IEC 61754-7-2 [11] see Figure 19. Note: This specification uses the terms MPO-12 in place of the TIA term MPO and MPO-12 Two Row in place of the TIA term MPO Two Row.

Aligned keys are used to ensure alignment between the modules and the patchcords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top. Note: Two alignment pins are present in each receptacle.



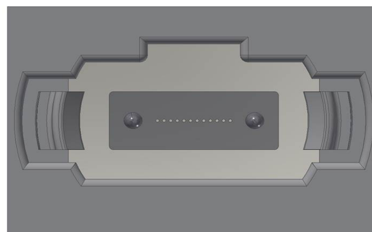
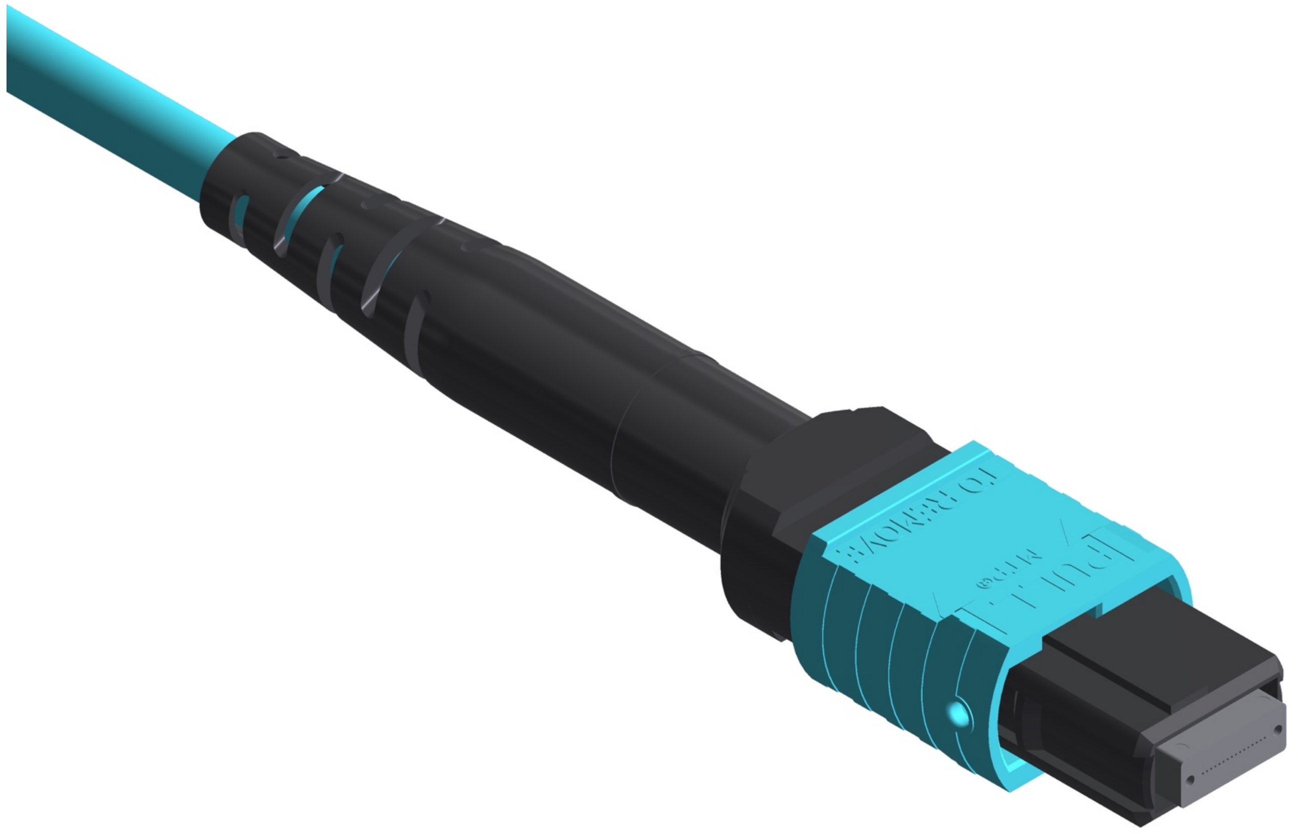


Figure 17: MPO-12 One row optical patchcord and module receptacle



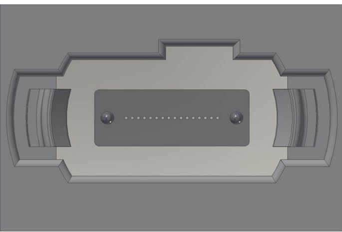
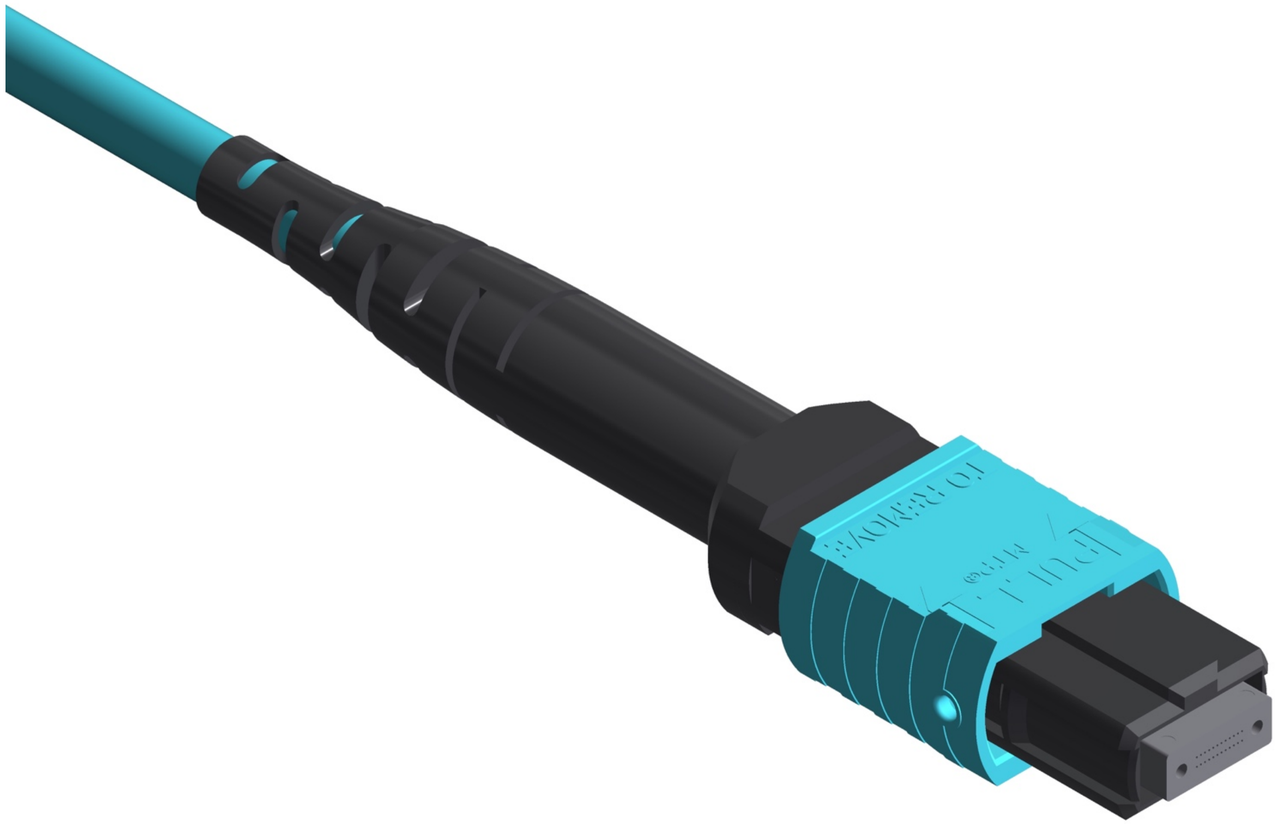


Figure 18: MPO-16 One row optical patchcord and module receptacle



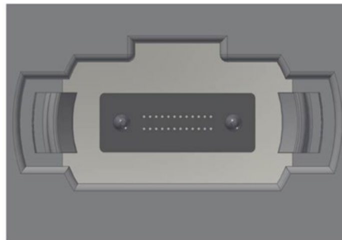


Figure 19: MPO-12 Two row optical patchcord and module receptacle

5.2.2 Duplex LC Optical Cable connection

The Duplex LC optical plug and module receptacle are specified in TIA-604-10 [24] and IEC 61754-20 [13], and shown in Figure 20.

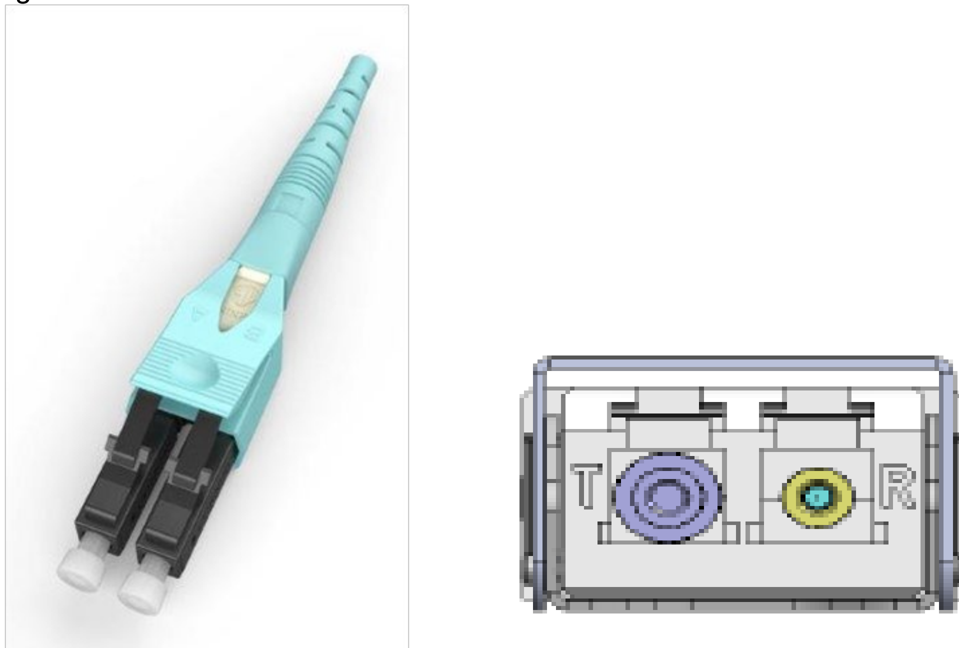


Figure 20: Duplex LC optical patchcord and module receptacle

5.2.3 Dual CS Optical Cable connection

The Dual CS optical receptacle for a QSFP-DD/QSFP-DD800/QSFP-DD1600 modules are specified in TIA-604-19 [27] and shown in Figure 21.

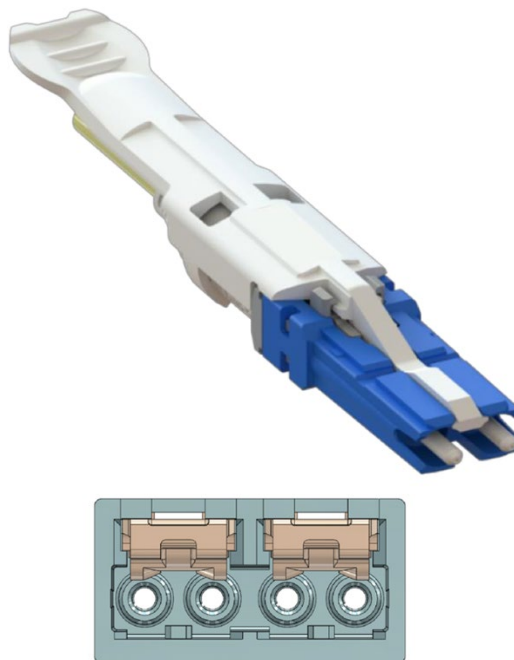


Figure 21: Dual CS connector optical patchcord and module receptacle

5.2.4 Quad SN Optical Cable connections

The Quad SN optical connector and receptacle for QSFP-DD/QSFP-DD800/QSFP-DD1600 module is specified in SN-60092019 [22] and shown in Figure 22. The top key and offset bottom key are used to ensure alignment between the modules and the patch cords.

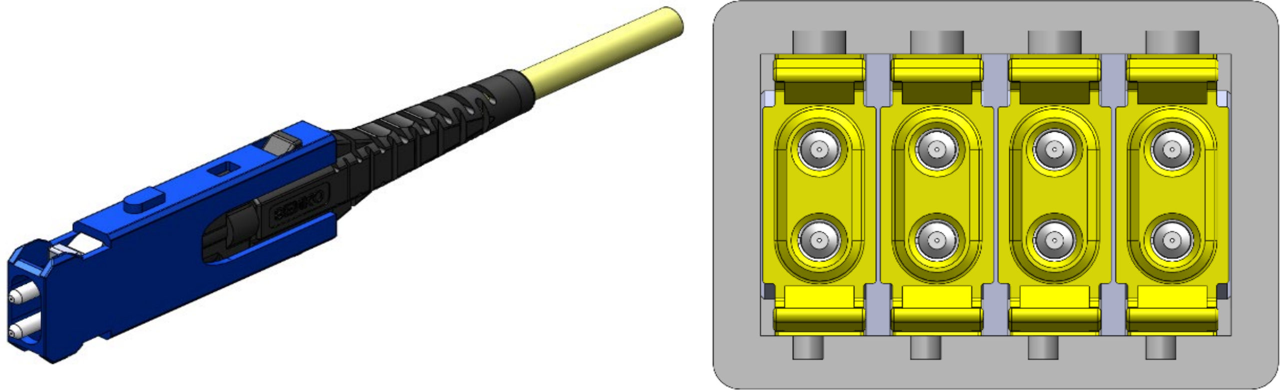


Figure 22: Quad SN optical connector pathcord and four-port module receptacle

5.2.5 Quad MDC Optical Cable connection

The Quad MDC optical plug and receptacle for a QSFP-DD/QSFP-DD800/QSFP-DD1600 modules are specified in USC-11383001 [28] and shown in Figure 23. The optical connector is orientated such that the keying feature of the MDC receptacle is on the top.

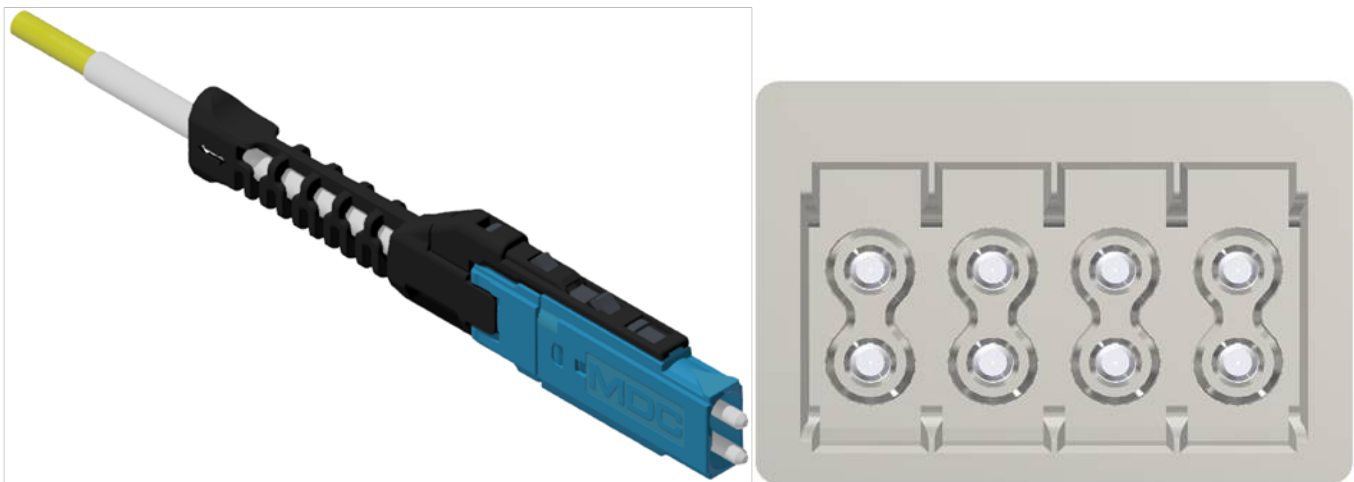


Figure 23: Quad MDC optical connector patchcord and four-port module receptacle

5.2.6 Dual SN Optical Cable connections

The Dual SN optical connector and receptacle for QSFP-DD/QSFP-DD800/QSFP-DD1600 modules are specified in SN-60092019 [22] and shown in Figure 24. The top key and offset bottom key are used to ensure alignment between the modules and the patch cords.

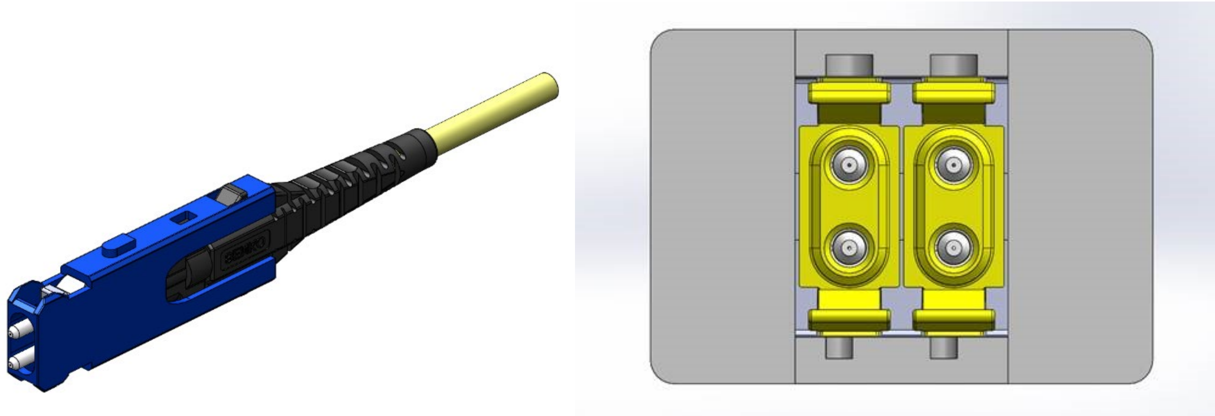


Figure 24: Dual SN optical connector patchcord and dual-port module receptacle

5.2.7 Dual MDC Optical Cable connection

The Dual MDC optical plug and receptacle for a QSFP-DD/QSFP-DD800/QSFP-DD1600 modules are specified in USC-11383001 [28] and shown in Figure 25. The optical connector is orientated such that the keying feature of the MDC receptacle is on the top.

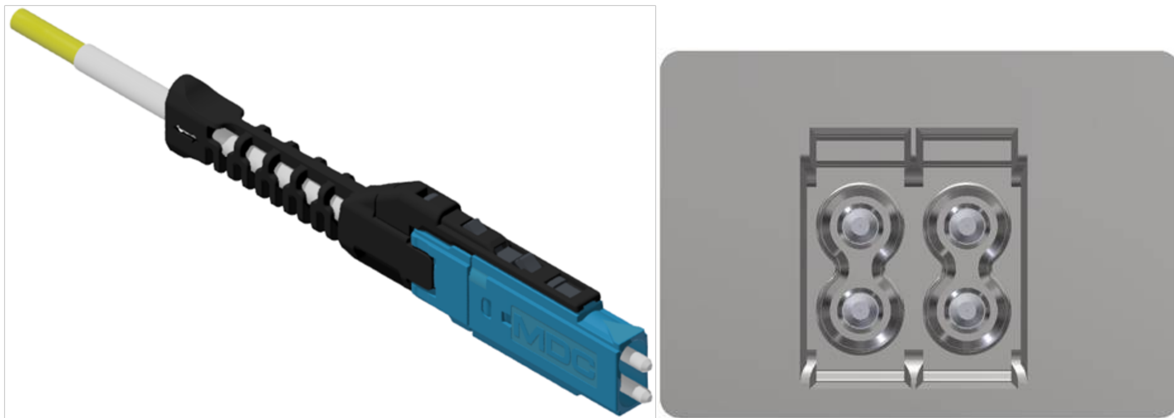


Figure 25: Dual MDC optical connector patchcord and dual-port module receptacle

5.2.8 Dual Duplex LC Optical Cable connection

The Dual Duplex LC module receptacle for a QSFP-DD Type 2B Module is shown in Figure 27. Each LC Duplex interface is specified in TIA-605-10 [25], and the two LC Duplex ports need to be pitched from 7.3 mm to 7.5 mm apart (Figure 32). The latches of LC plug may exceed the overall module width (see Figure 28). The pitch between the cages in a system design will need to accommodate this excess width but it is not expected that this will reduce port counts in a system.

Note: The dual duplex LC latch width of 23 mm is an informative dimension. The duplex LC pitch dimension 6.25 mm is a basic dimension defined by TIA-604-10 [25] and IEC 61754-20 [13].

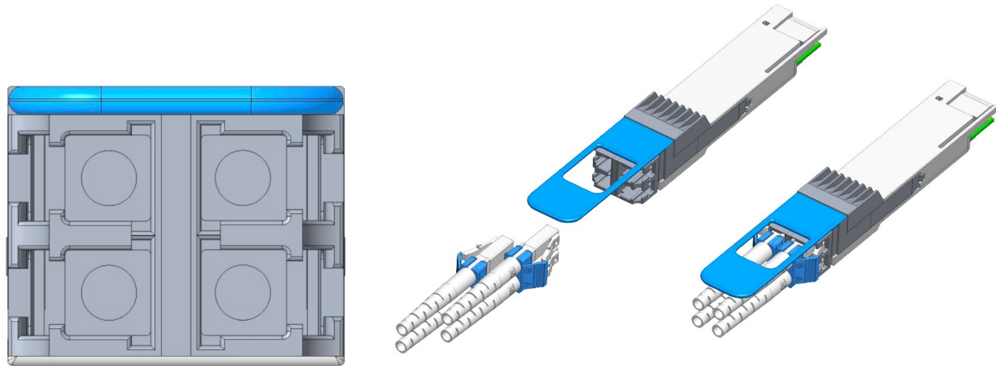


Figure 26: Dual Duplex LC module receptacle (in support of breakout applications)

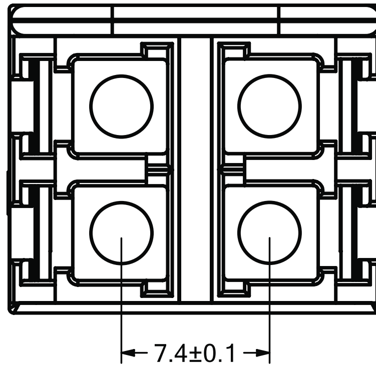


Figure 27: Dual Duplex LC module receptacle port pitch

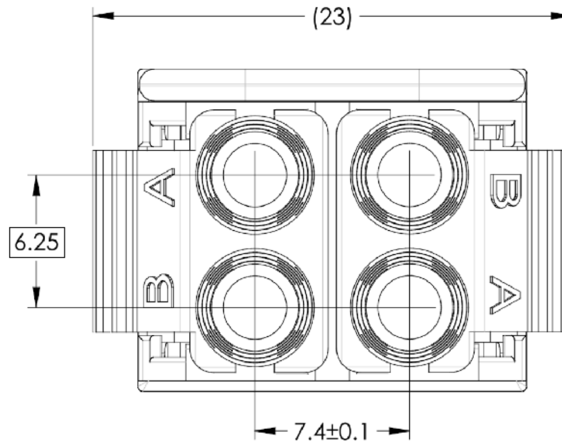


Figure 28: Dual Duplex LC latch width

5.2.9 Dual MPO-12 Optical Cable connection

The Dual MPO-12 module receptacle for a QSFP-DD Type 2B module is shown in Figure 29. Each MPO-12 interface is specified in TIA-604-5 [24], and the two MPO-12 ports need to be pitched at least 9.4 mm apart (Figure 30).'

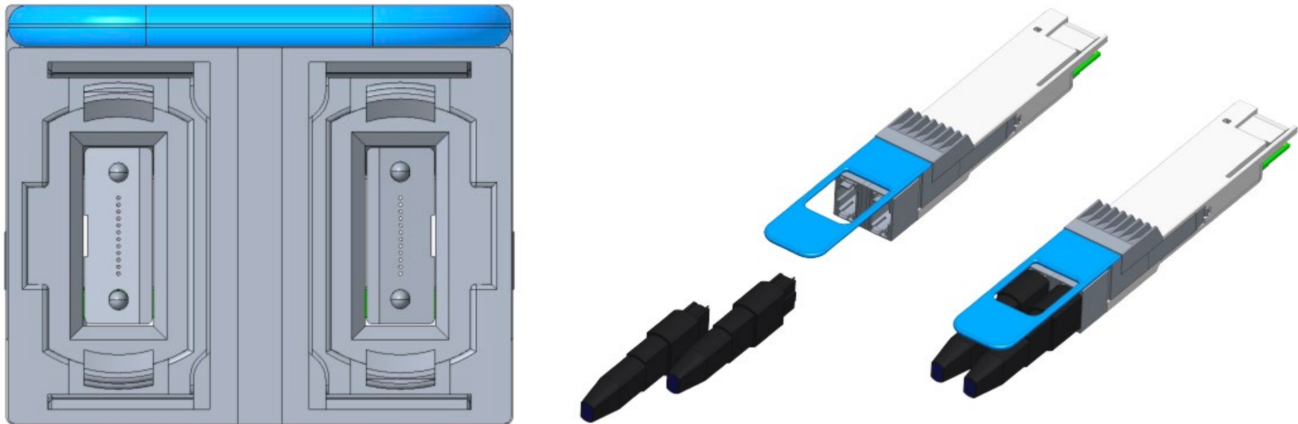


Figure 29: Dual MPO module receptacle (in support of breakout applications)

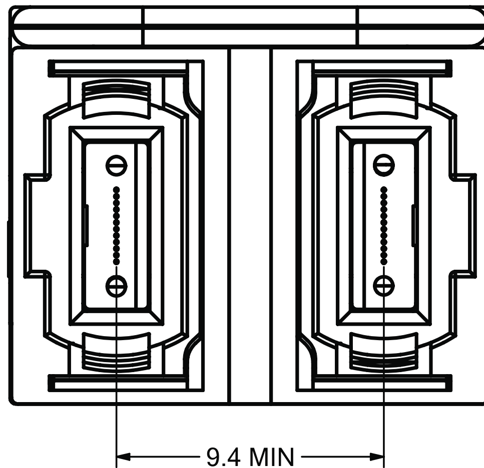


Figure 30: Dual MPO-12 module receptacle port pitch

5.3 Module Color Coding and Labeling

An exposed feature of the QSFP-DD/QSFP-DD800/QSFP-DD1600 module (a feature or surface extending outside of the bezel) should be color coded as follows:

Beige for 850nm
Blue for 1310nm
White for 1550nm

Above color coding list is not exhaustive, other specifications may define additional color codes to supplement or override above color coding as needed.

Each QSFP-DD/QSFP-DD800/QSFP-DD1600 module shall be clearly labeled. The complete labeling need not be visible when the QSFP-DD/QSFP-DD800/QSFP-DD1600 module is installed. QSFP-DD recess bottom area is the recommended location of the label, but the location of label for QSFP-DD800/QSFP-DD1600 is on the module nose surface. Labeling shall include:

Appropriate manufacturing and part number identification
Appropriate regulatory compliance labeling
A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

Optical wavelength
Required fiber characteristics (i.e., MMF/SMF)
Operating data rate
Interface standards supported
Link length supported
Connector Type

If required to comply with 9.3, a label must be applied to the top external surface of the module case, warning of high touch temperature.

The labeling shall not interfere with the mechanical, thermal or EMI features.

6 QSFP-DD Mechanical and Board Definition

This chapter is the foundation for QSFP-DD, QSFP-DD800 (see chapter 7), and QSFP-DD1600 (see chapter 0) modules specifications. Below is the list of relevant sections applicable to QSFP-DD800 and QSFP-DD1600 in addition to QSFP-DD:

- 6.1 Introduction to QSFP-DD/QSFP-DD800/QSFP-DD1600 Modules
- 6.2 Datums, Dimensions and Component Alignment
- 6.3 Module Form Factors for QSFP-DD/QSFP-DD800
- 6.4 Module Flatness and Roughness 6.1
- 6.6 Module Extraction and Retention Forces.

6.1 Introduction to QSFP-DD/QSFP-DD800/QSFP-DD1600 Modules

The cages and modules defined in this chapter are illustrated in Figure 31 (2x1[1] stacked cage and module), Figure 32 (press fit cage for surface mount connector), and Figure 33 (illustrate Type 1, Type 2, Type 2A, 2B, and Type 2C pluggable modules). All pluggable modules and direct attach cable plugs (both Type 1 and Type 2) must mate to the connectors and cages defined in this specification. The Type 2 module allows an additional extension of the module outside of the cage to allow for flexibility in module design. A Type 2A, 2B, and Type 2C modules include a heat sink on the extension of the module outside the cage to provide enhanced thermal performance. Modules heatsink and retention clip thermal designs are application specific and not specifically defined by this specification. QSFP-DD/QSFP-DD800/QSFP-DD1600 module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Recommended riding heat sink normal force for power class 5 or higher is at least 25 N.

See Appendix B for informative recommendations on overall module length including handle. See Appendix C for recommended QSFP-DD heatsink on module extension design for Type 2A and 2B modules, Type 2B and Type 2C modules are only for QSFP-DD800/QSFP-DD1600 operation. See Appendix D for alternate QSFP-DD800/QSFP-DD1600 heatsink design for Type 2A module.

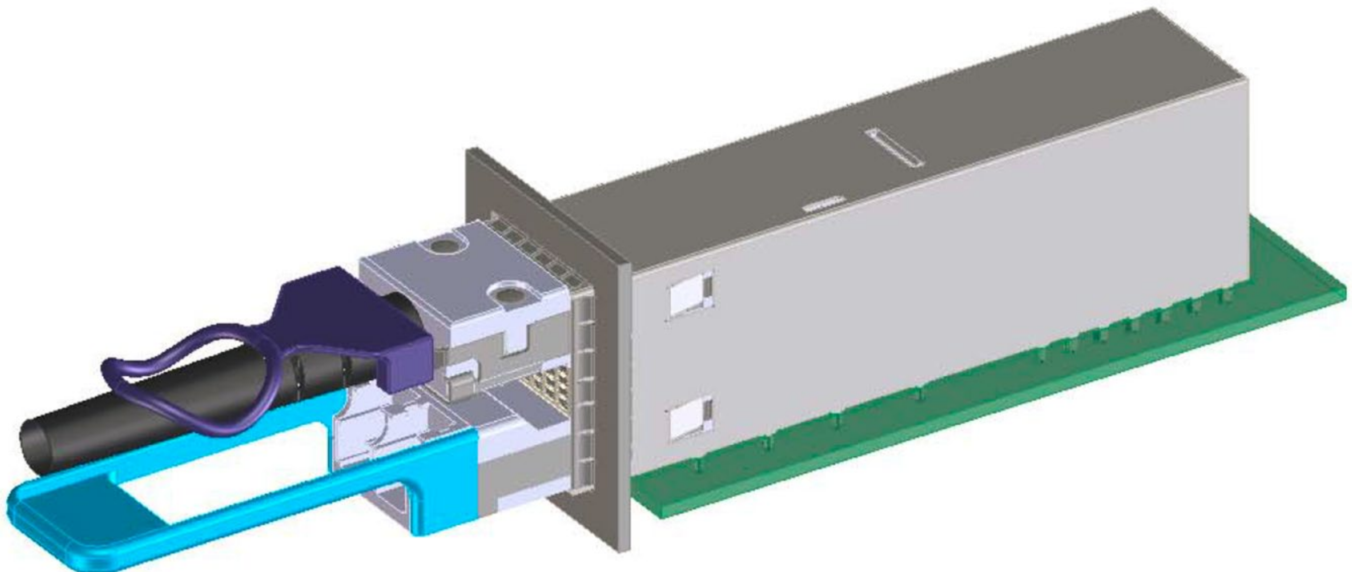


Figure 31: 2x1 stacked cage and module

[1] For QSFP-DD1600 currently only 1x1 SMT cage is defined.

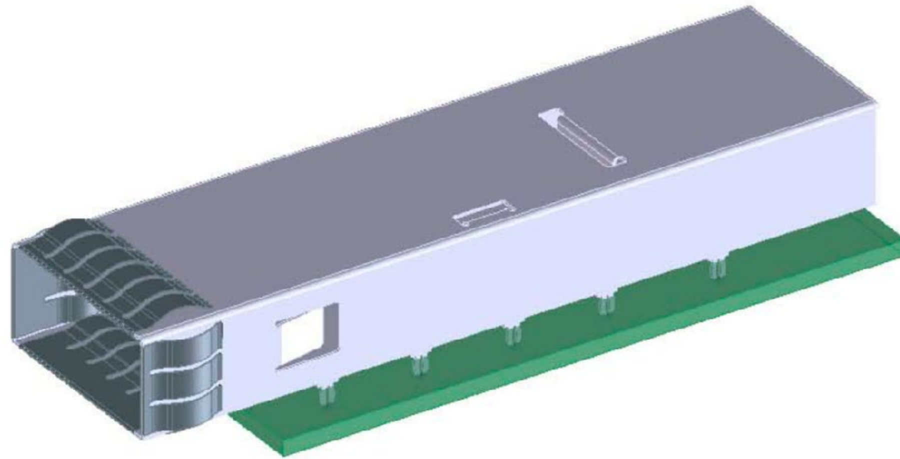


Figure 32: Press fit cage for surface mount connector

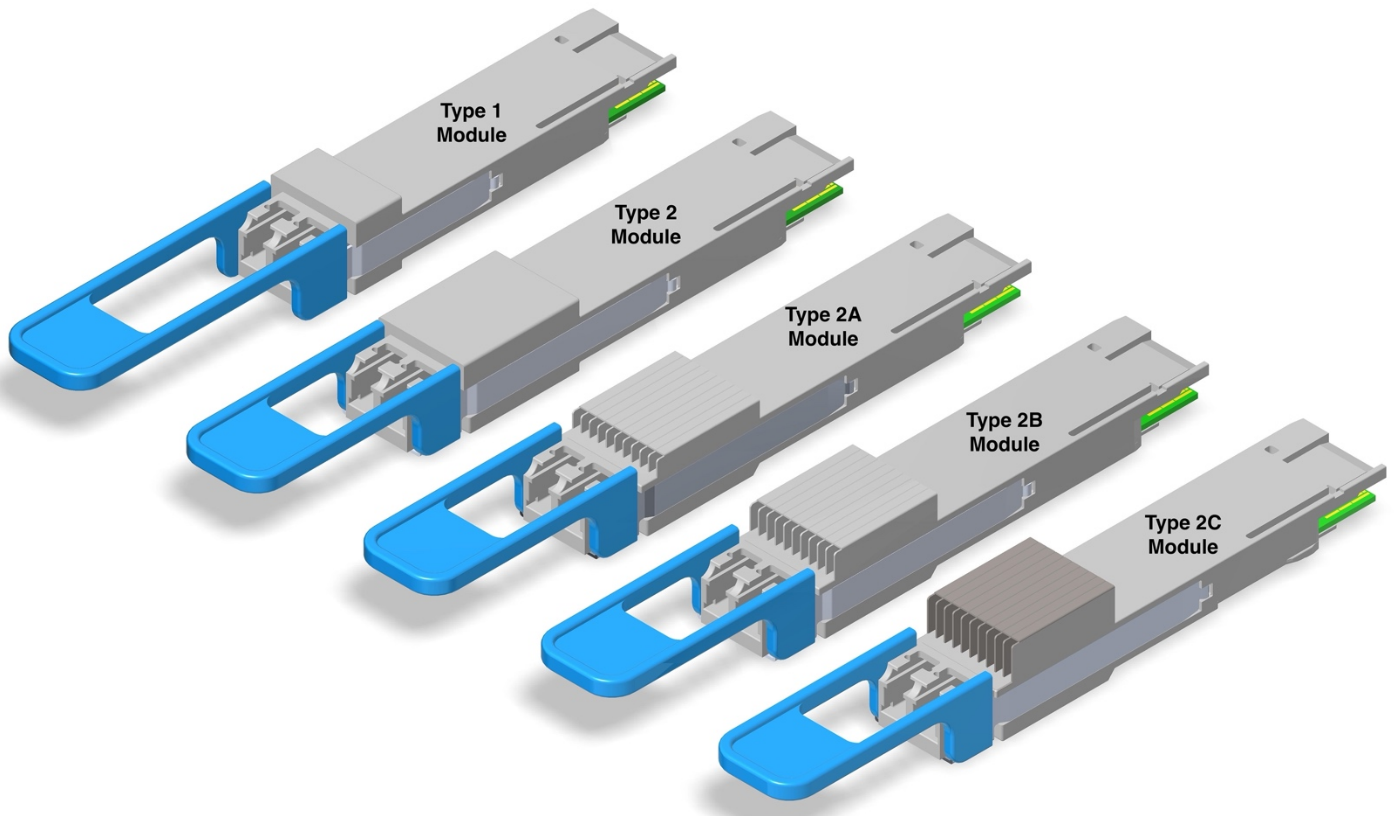


Figure 33: Type 1, Type 2, Type 2A, 2B, and Type 2C pluggable modules

1

2 ## 6.2 Datums, Dimensions and Component Alignment

3 A listing of the QSFP-DD/QSFP-DD800/QSFP-DD1600 datums for the various components is contained in
4 Table 16. The alignments of some of the datums are noted. To reduce the complexity of the drawings, all
5 dimensions are considered centered unless otherwise specified. Dimensions and tolerancing conform to ASME
6 Y14.5-2009 [4]. All dimensions are in millimeters.

7

8 **Table 16- Datums**

Datum[1]	Description
A	Host Board Top Surface
B	Inside surface of bezel
C	Distance between Connector terminal thru holes on host board[3]
D	Hard stop on module[2]
E	Width of module[3]
F	Height of module housing
G	Width of module pc board[3]
H	Leading edge of signal contact pads on module pc board
J	Top surface of module pc board
K	Host board thru hole #1 to accept connector guidepost[2]
L	Host board thru hole #2 to accept connector guidepost[2]
M	Width of bezel cut out[3]
P	Vertical Center line of internal surface of cage
S	Seating plane of cage on host board
T	Hard stop on cage[2]
AA	Connector slot width[3]
BB	Seating plane of connector on host board
DD	Top surface of module housing
EE	Centerline of module opening to locate paddle card Datum H
FF	Centerline of upper port cage height
GG	Centerline of lower port cage height
EE	Primary Datum hole for 2x1 Host PCB
Notes: 1. All dimensions are in mm. 2. Datums D and T are aligned when assembled (see Figure 34 and Figure 35). 3. Centerlines of datums AA, C, E, G, M are aligned on the same vertical plane.	

9

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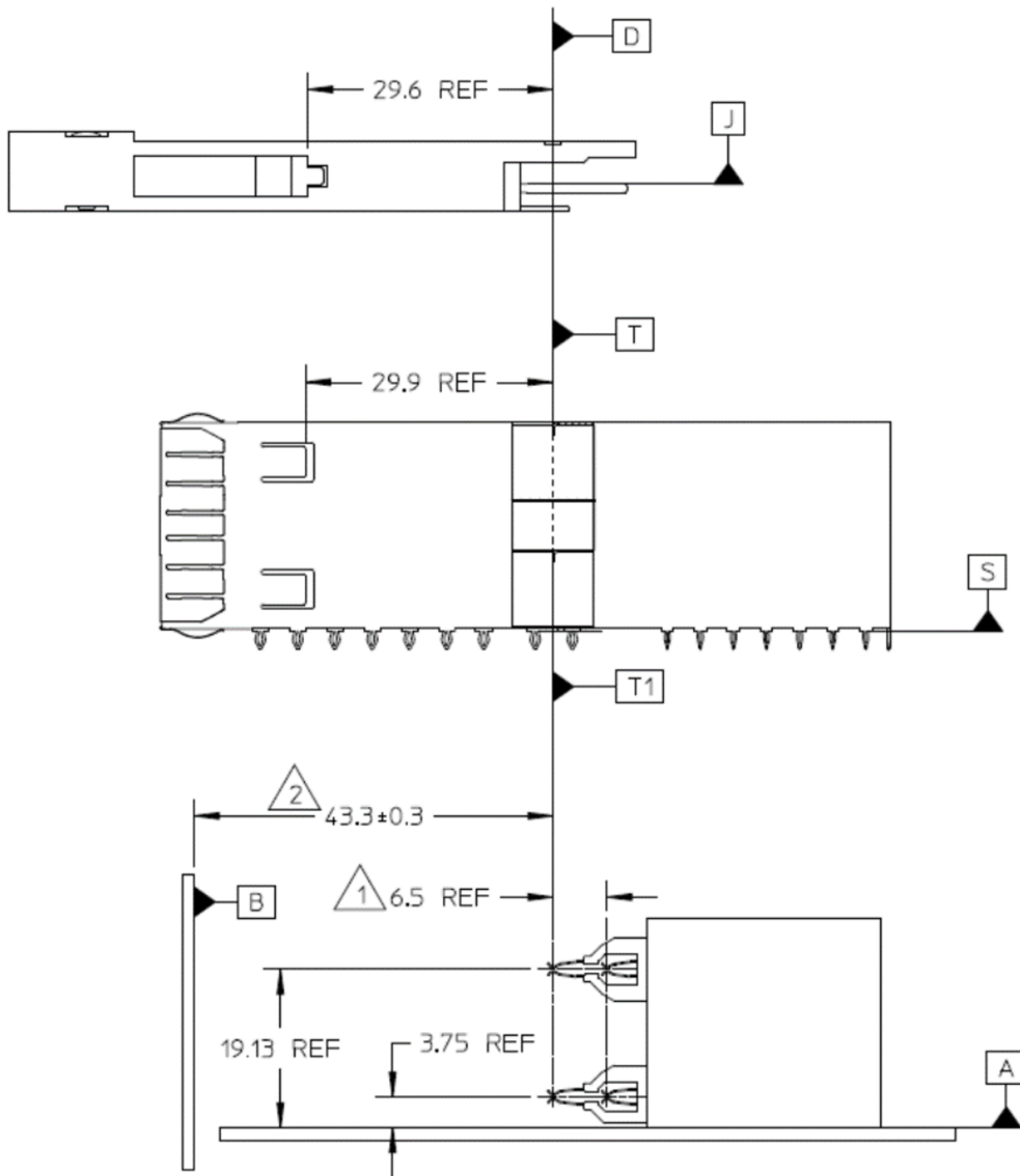


Figure 34: 2X1 stacked press fit connector/cage datum descriptions

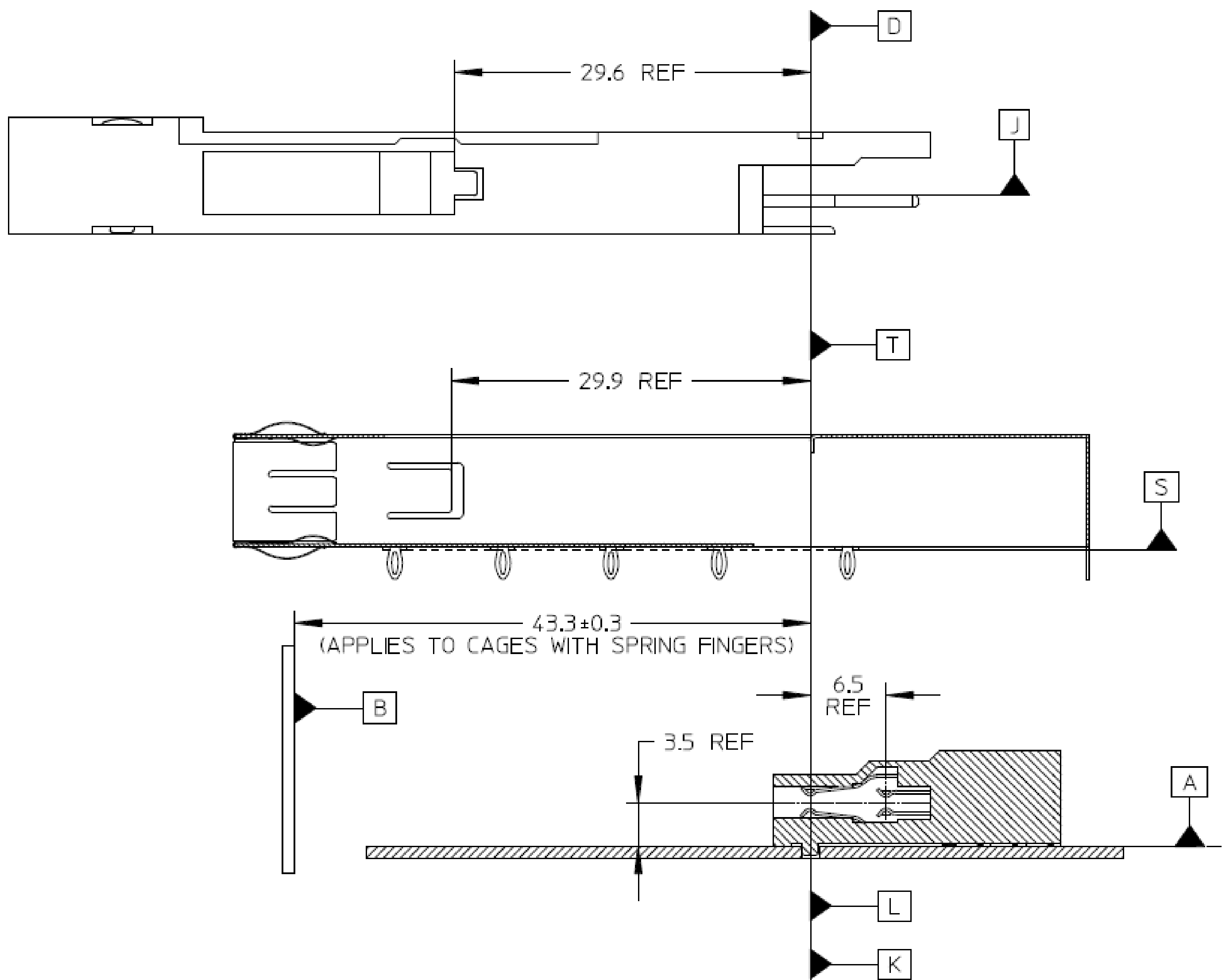
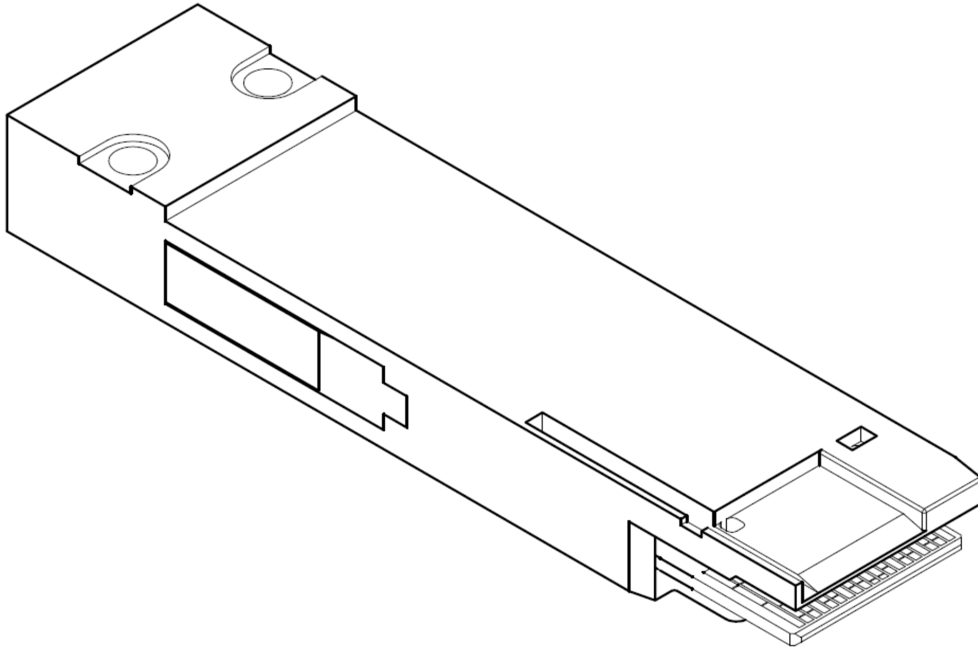


Figure 35: Surface mount connector/cage datum descriptions

6.3 Module Form Factors for QSFP-DD/QSFP-DD800/QSFP-DD1600

The mechanical outline for the Type 1 module is shown in Figure 36, the Type 2 module is shown in Figure 37, the Type 2A module with nose heat sink is shown in Figure 38, and the Type 2B module with taller nose heat sink is shown in Figure 39. The module shall provide a means to self-lock with either the 2x1 stacked cage or SMT cage upon insertion. The module package dimensions are defined in Figure 42, Figure 43, and Figure 44. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 4.



1
2
3 **Figure 36: Type 1 module**
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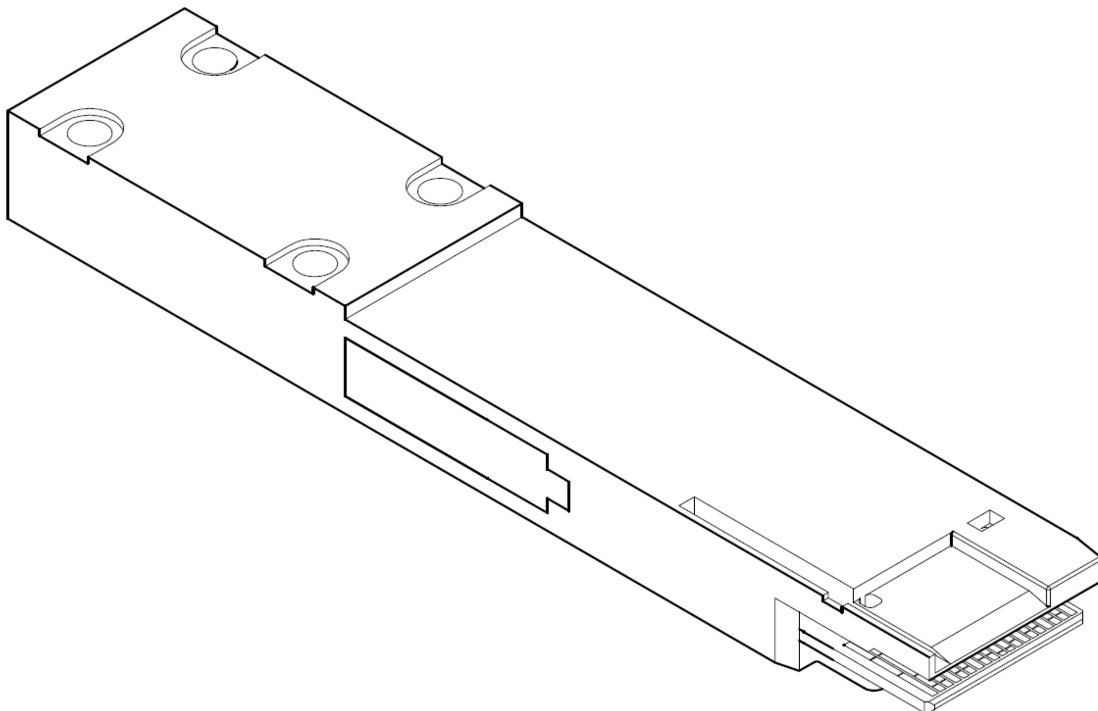

6
7 **Figure 37: Type 2 module**
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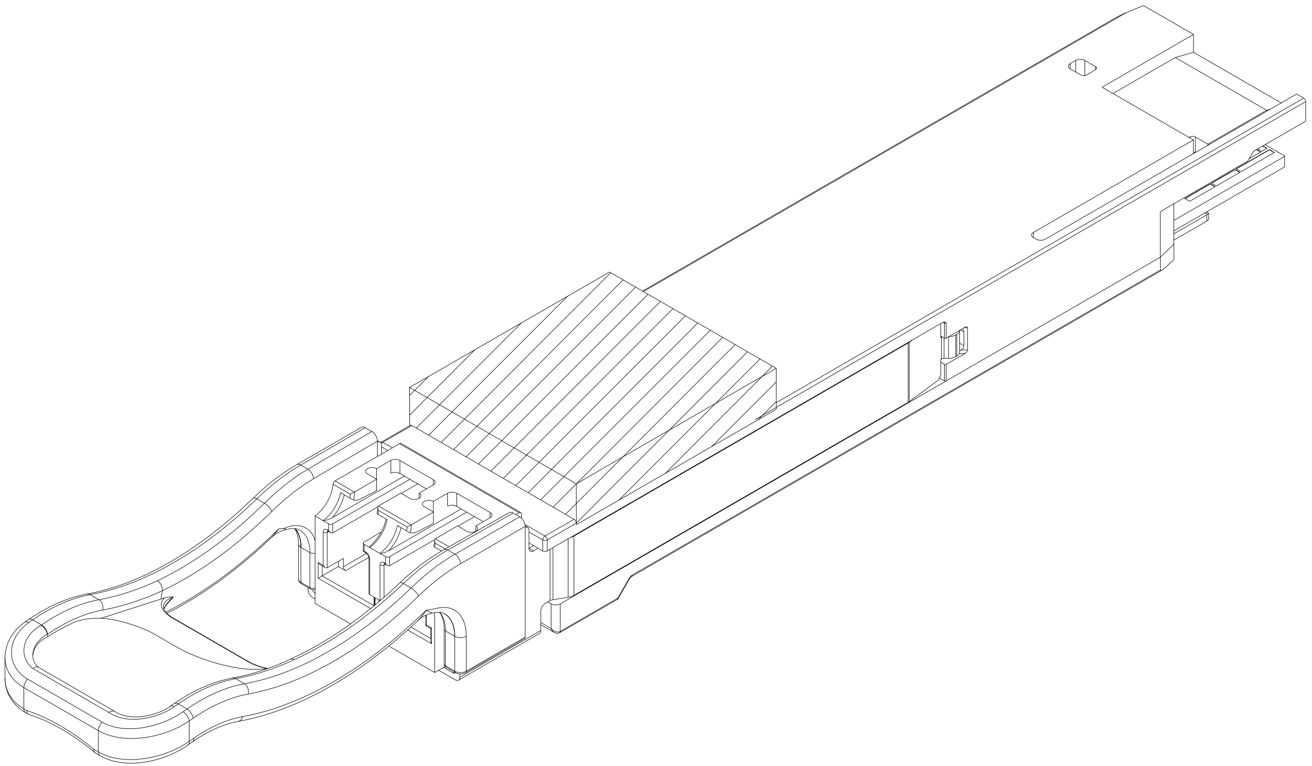
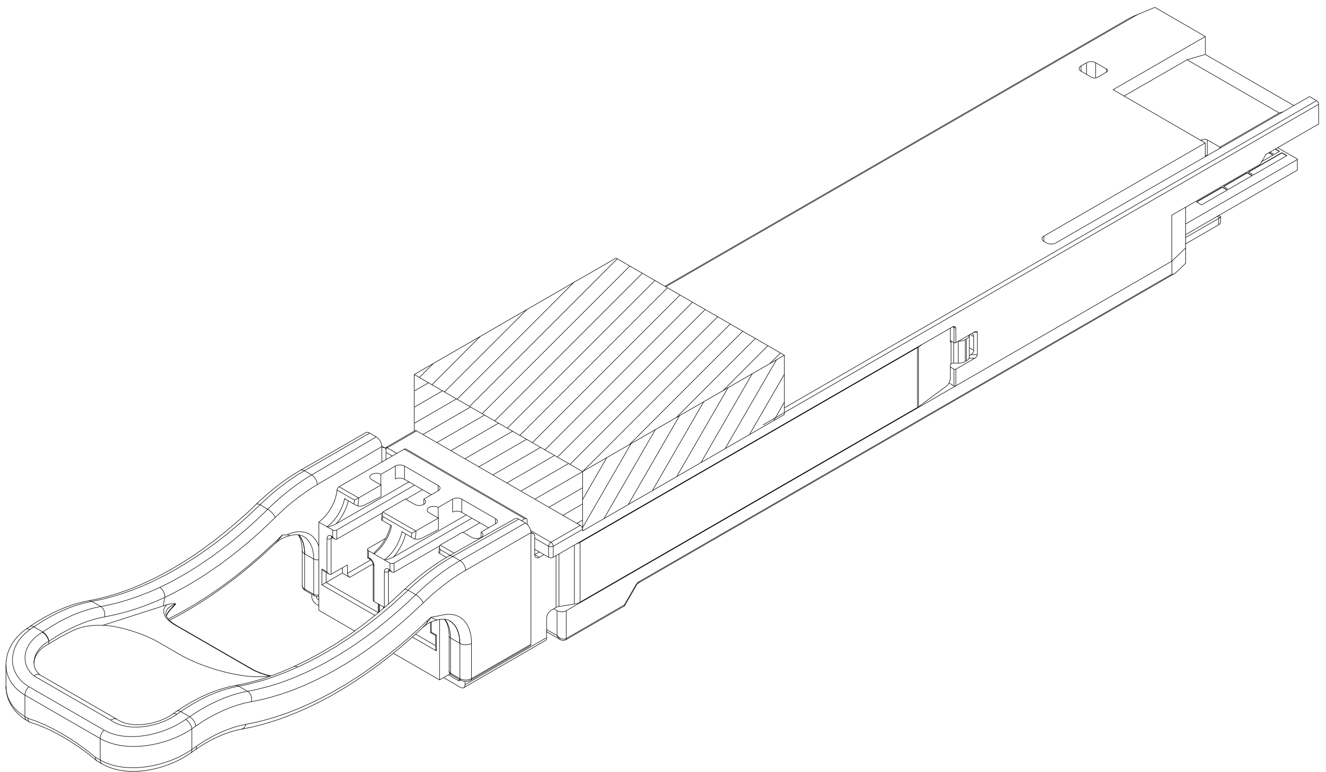


1
2 **Figure 38: Type 2A Module**



3
4 **Figure 39: Type 2B module**

5
6 Figure 39 Type 2B Module (Cannot be used in combination with the 2x1 Electrical Connector Mechanical in section 6.7
7 due to possible mechanical interference)

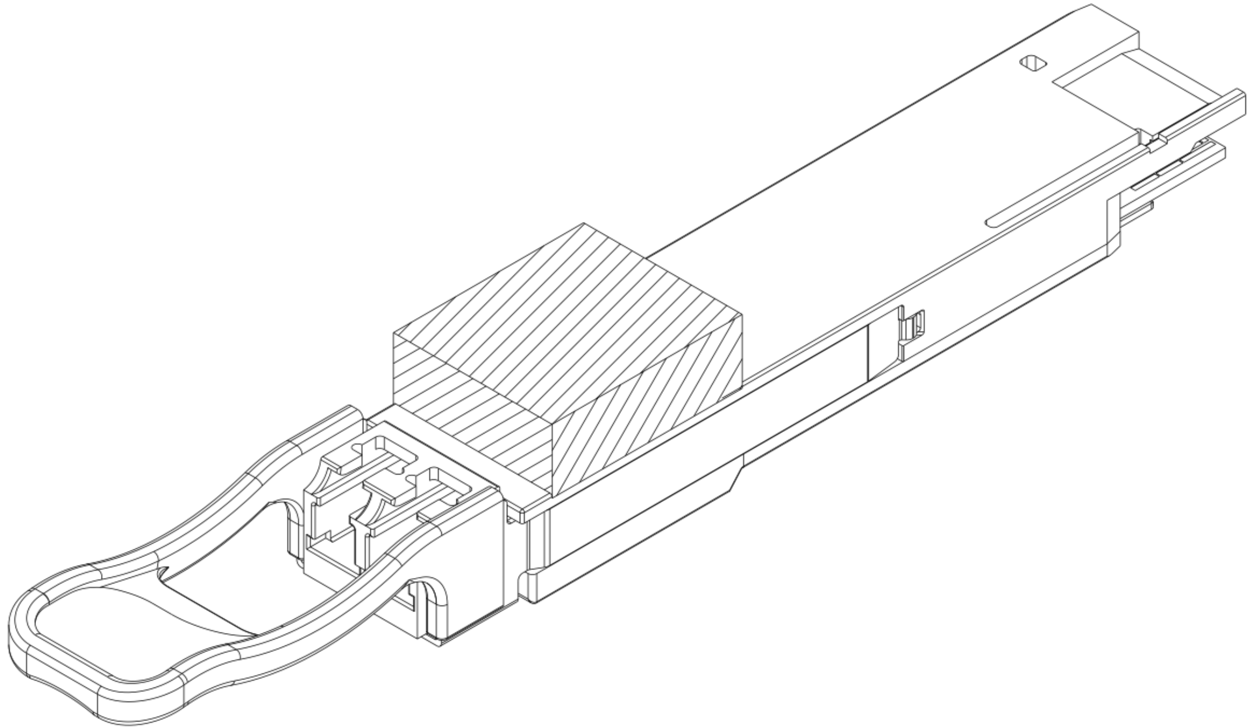


Figure 40: Type 2C module

Figure 40 Type 2C Module (Cannot be used in combination with the 2x1 Electrical Connector Mechanical in section 6.7 due to possible mechanical interference)

NOTES APPLY TO MODULE DRAWING

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. UNLESS OTHERWISE SPECIFIED, SHARP CORNERS AND EDGES ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS TO A MINIMUM RADIUS OF 0.20 MM.
4. DIMENSION DEFINES ENLARGED SECTION OF TRANSCEIVER THAT EXTENDS OUTSIDE OF CAGE TO ACCOMMODATE MATING PLUG AND ACTUATOR MECHANISM.
5. SURFACES ON ALL 4 SIDES OF THE 12.4 MIN DIMENSION TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.
6. DIMENSION APPLES TO LATCH MECHANISM.
7. DIMENSION APPLIES TO THE LOCATION OF THE EDGE OF THE MODULE BOARD PAD, DATUM H. CONTACTS 21, 22, 36 AND 37 ARE VISIBLE.
8. DIMENSION TO INCLUDE BAIL TRAVEL.
9. DIMENSION APPLY TO OPENINGS IN THE HOUSING.
10. OPTIONAL FEATURE TO AID INSPECTION OF DIMENSIONS FROM DATUM D.
11. FLATNESS AND SURFACE ROUGHNESS (Ra) APPLIES FOR INDICATED LENGTH AND MIN WIDTH OF 13MM. SURFACE TO BE THERMALLY CONDUCTIVE. SEE SECTION 6.4, TABLE 17 AND TABLE 18 FOR FLATNESS AND ROUGHNESS REQUIREMENTS.
12. HIGHER WATTAGE MODULES MAY REQUIRE ADDITIONAL SPACE FOR COOLING.
13. BLOCKING FEATURE IS CRITICAL TO APPLICATION FUNCTION. A RADIUS OF 0.2 ± 0.05 MM IS REQUIRED ON THE LEADING EDGES OF THIS FEATURE.
14. NO LABEL SHALL BE APPLIED IN THIS AREA. ETCHINGS ARE ALLOWED BUT MUST NOT AFFECT THERMAL PERFORMANCE..
15. THE LABEL(S) SHALL NOT INTERFERE WITH THE MECHANICAL, THERMAL, OR EMI PERFORMANCE AND MUST NOT VIOLATE NOTE 5.
16. DIMENSION APPLIES TO LATCH POCKET
17. OPTIONAL FEATURE TO AID IN TOOLING STRENGTH.

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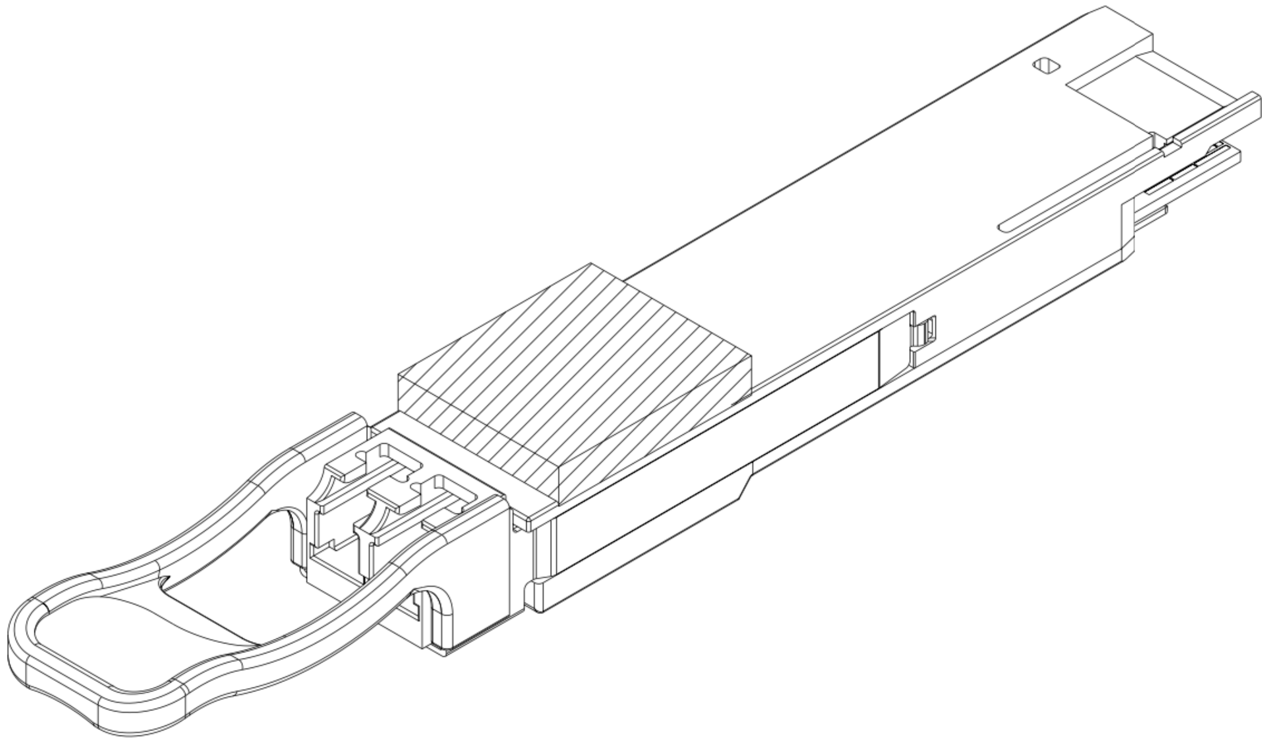
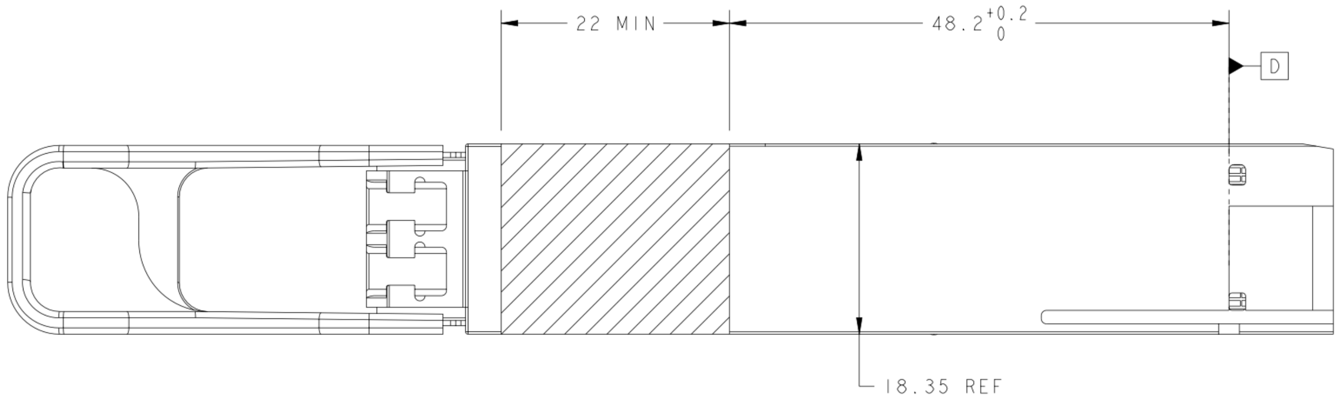




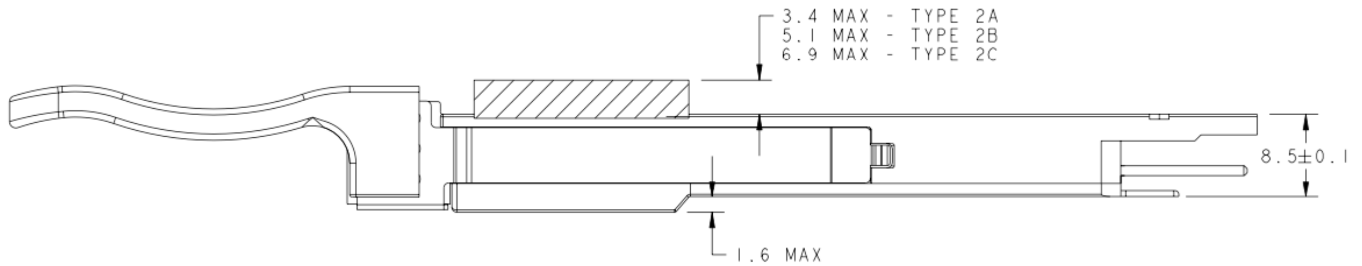
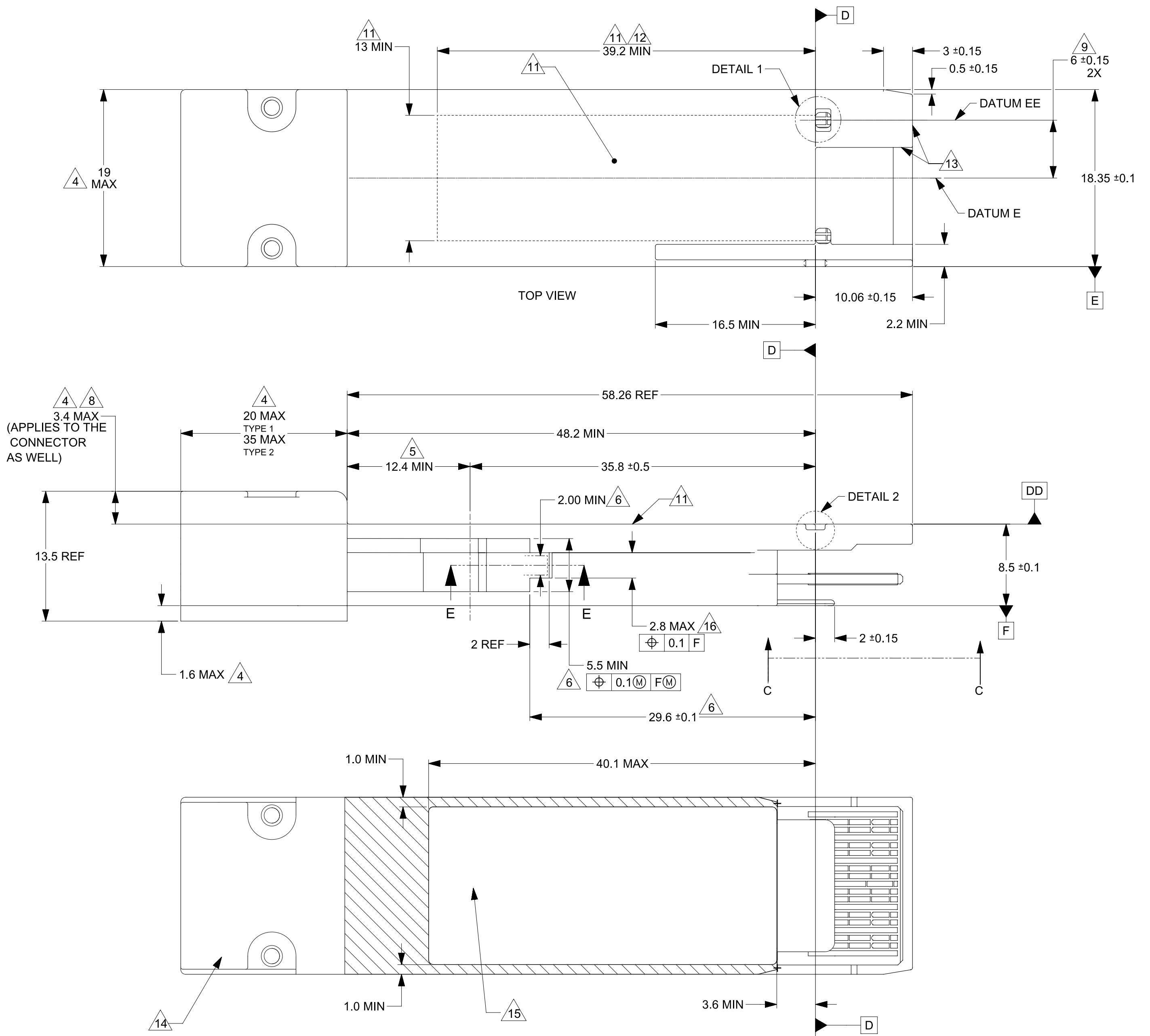
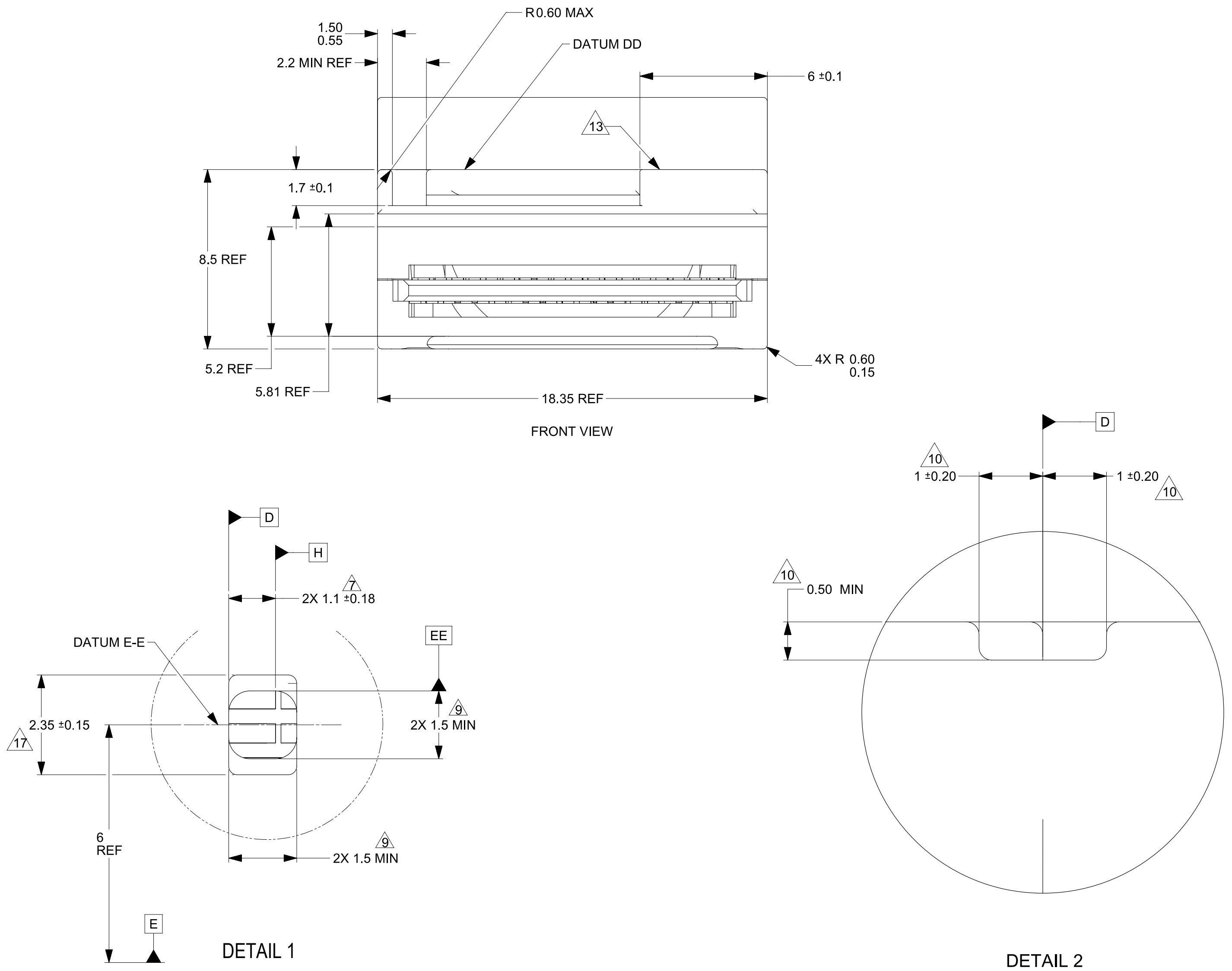


Figure 41: Type 2A, 2B, and 2C Module with heat sink

1



2
3 **Figure 42: Drawing of the QSFP-DD module**
4



1
2
3 **Figure 43: Drawing of QSFP-DD module end face**
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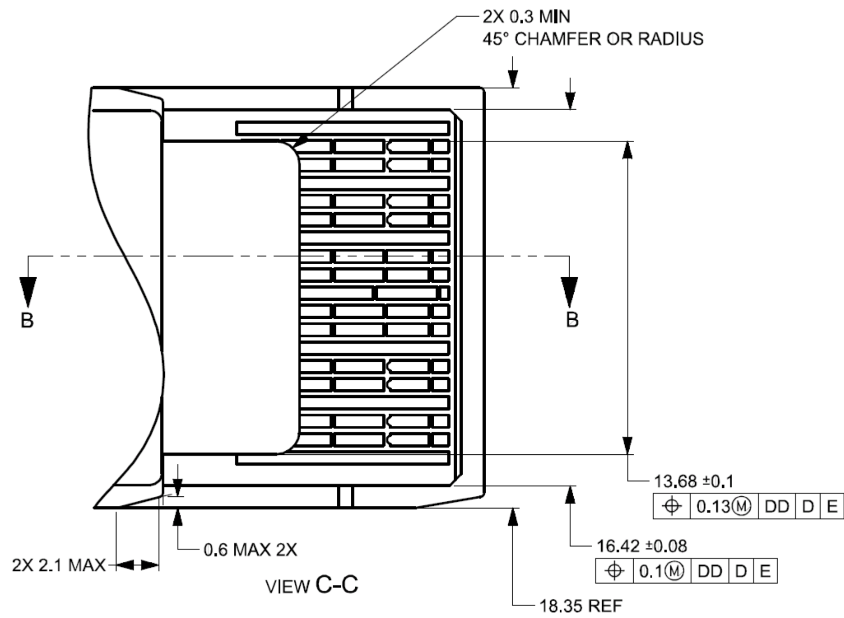
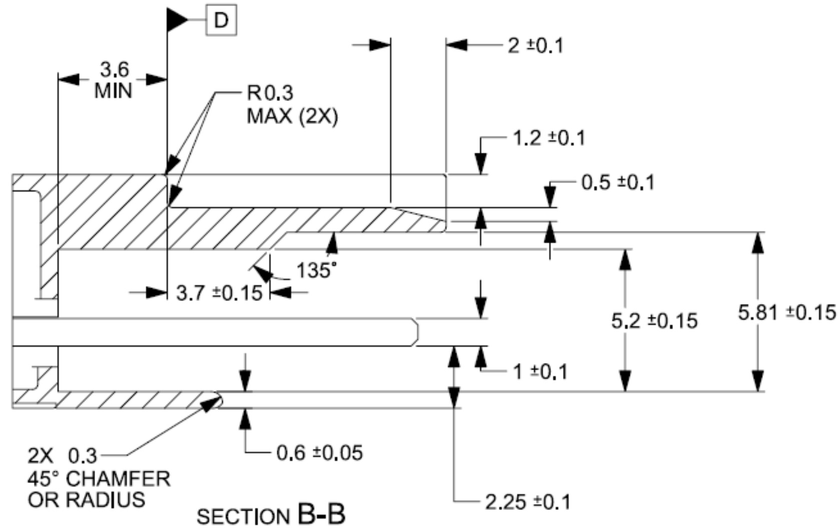
5
6



1



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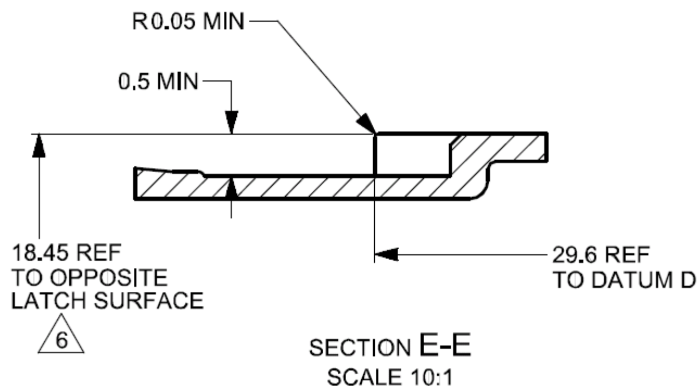
3



4
5
6 **Figure 44: Detailed dimensions of the QSFP-DD module opening**
7

6.4 Module Flatness and Roughness

QSFP-DD/QSFP-DD800/QSFP-DD1600 module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area for QSFP-DD by Figure 42 and Figure 43 and for QSFP-DD800 by Figure 63. Specifications for QSFP-DD/QSFP-DD800/QSFP-DD1600 Module flatness and surface roughness are shown in Table 17 (see Figure 42 and Figure 63 note 11). Flatness and roughness specifications applies to both top and bottom surfaces of the modules. Power class 1Cu is dedicated to passive copper cables with a more relaxed flatness of 0.15 mm.

Table 17- QSFP-DD modues formfactor flatness specifications

Power Class[1]	Module Flatness (mm)	Surface Roughness (Ra, µm)
1Cu[2]	0.15	1.6
1	0.075	1.6
2	0.075	1.6
3	0.075	1.6
4	0.075	1.6
5	0.050	0.8
6	0.050	0.8
7	0.050	0.8
8	0.050	0.8

1. QSFP-DD/QSFP-DD800/QSFP-DD1600 power classes are defined in Table 12.
2. Power class 1Cu maximum power dissipation is the same as power class 1.

To improve thermal performance, optional enhanced surface specifications are specified in Table 18. This is an optional specification and does not override the required specifications in Table 17.

Table 18- Optional Enhanced Module flatness specifications

Power Class	Module Flatness (mm)	Surface Roughness (Ra, µm)
8	0.025	0.4

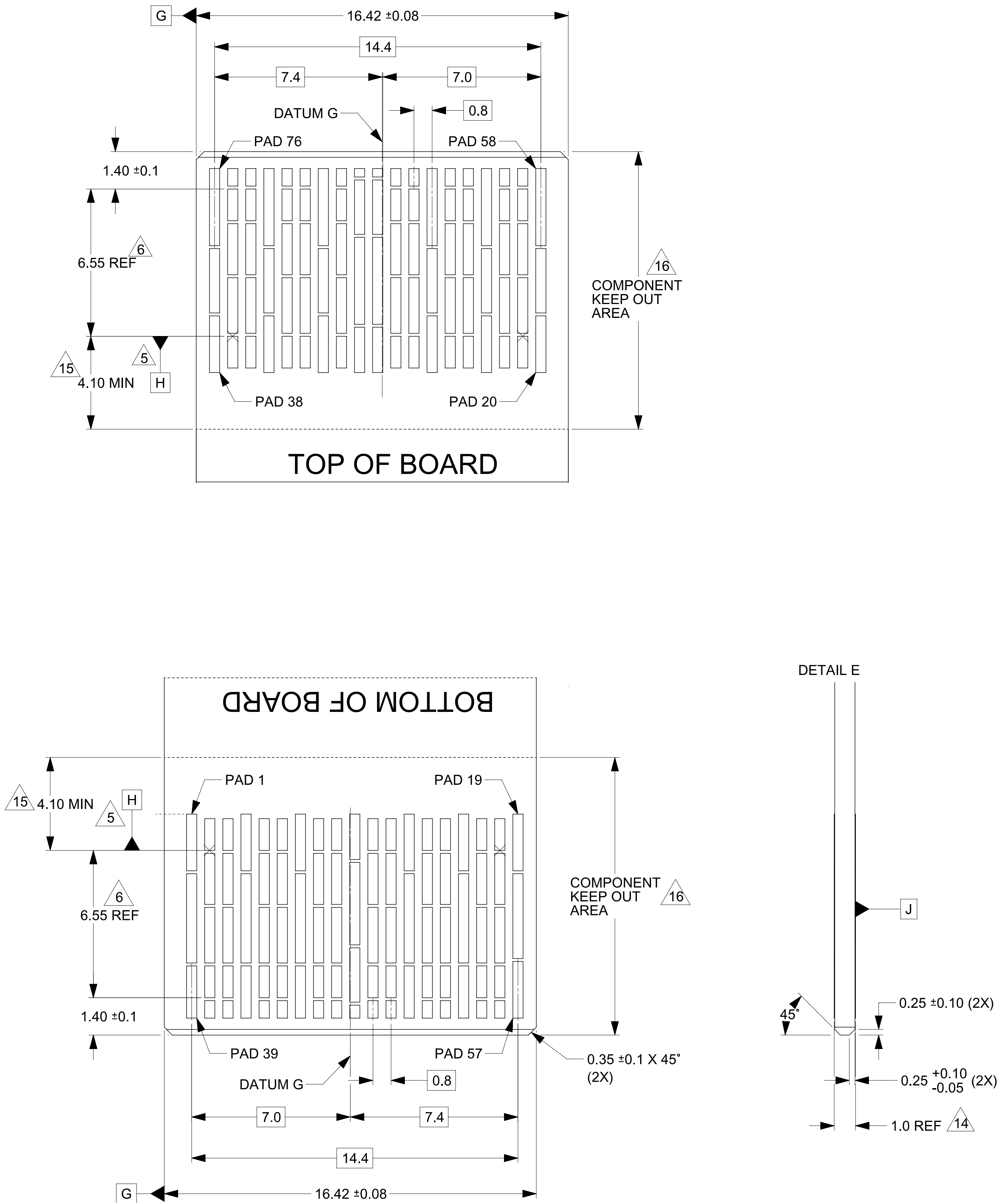
1
6.5 QSFP-DD module paddle card dimensions notes
2 Notes for module paddle cards drawings applies to Figure 45 and Figure 46.
3

NOTES APPLY TO MODULE PADDLE CARD:

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD
5. DATUM H IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTERMOST SIGNAL CONTACT PADS TO BE RE-ESTABLISHED ON EACH SIDE
6. DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS
7. DIMENSION AND TOLERANCE APPLIES TO ALL GROUND PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
8. DIMENSION AND TOLERANCE APPLIES TO ALL POWER PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
9. DIMENSION AND TOLERANCE APPLIES TO ALL SIGNAL PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
10. A ZERO GAP IS ALLOWED FOR A CONTINIOUS SIGNAL PADS ON BOTH TOP AND BOTTOM
11. APPLIES TO ALL SIGNAL PAD TO PRE-WIPE SPACING
12. PRE-WIPE PADS (SHADED AREA), ON MODULE CARD HOST ARE OPTIONAL
13. PRE-WIPE PADS (UNSHADED AREA), ARE REQUIRED EXCEPT IN CONTINUOUS POWER AND GROUND DESIGNS
14. PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS MUST NOT BE PROUD OF THE PAD SURFACE
15. MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS
16. COMPONENT KEEP OUT AREA MUST MEASURE FROM DATUM H
17. A SINGLE, DOUBLE AND TRIPLE SPLIT IN THE PRE-WIPE SIGNAL PAD IS OPTIONAL. AND IF IMPLEMENTED THE RESULTING 2, 3, AND 4 PADS SHALL BE SEPARATED WITH A GAP OF 0.13+/- 0.05
18. CONTACT PAD PLATING
    - 0.38 MICROMETERS MINIMUM GOLD OVER
    - 1.27 MICROMETERS MINIMUM NICKEL

    ALTERNATE CONTACT PAD PLATING
    - 0.05 MICROMETERS MINIMUM GOLD OVER
    - 0.30 MICROMETERS MINIMUM PALLADIUM OVER
    - 1.27 MICROMETERS MINIMUM NICKEL

4



1
2
Figure 45: Module paddle card dimensions

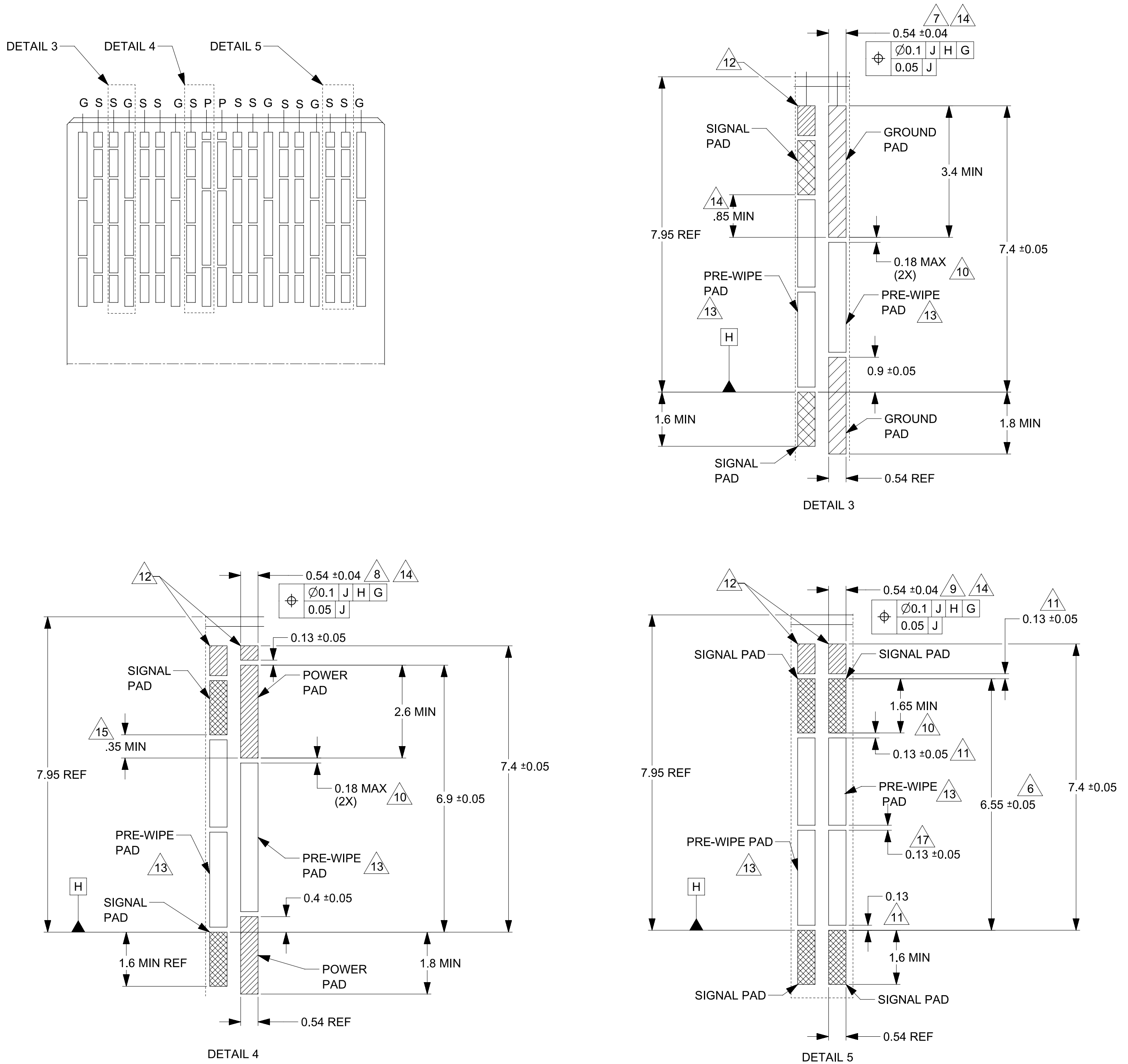


Figure 46: Detail module pad dimensions

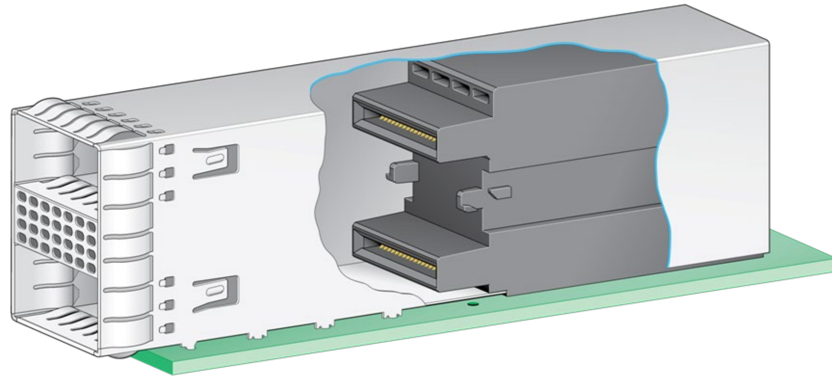
6.6 Module Extraction and Retention Forces

The normative requirements for QSFP-DD/QSFP-DD800/QSFP-DD1600 insertion forces, extraction forces and retention forces are specified in Appendix A. The contact pad plating shall meet the requirements in 6.5.

6.7 QSFP-DD 2x1 Stacked Electrical Connector Mechanical

Each of the QSFP-DD stacked connectors are a 76-contacts right angle connector. The integrated connector in a 2x1 stacked cage is shown in Figure 47 with detailed drawings in Figure 48, Figure 49 and Figure 50.

1 Recommendations for the 2x1 stacked cage bezel opening are shown in Figure 51. Recommended host PCB
2 layout are shown in Figure 53 and Figure 54.
3



4
5 **Figure 47: Integrated connector in the 2x1 stacked cage**

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

△3 DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED

△4 CONNECTOR REMOVED FOR CLARITY

△5 APPLIES TO ALL SPRING FINGERS ON ALL SIDES

△6 EXTERNAL CAGE DIMENSIONS DOES, NOT INCLUDE FOLDING TABS

△7 LENGTH OF CAGE AND SIGNAL TAILS

△8 PRESS FIT CAGE PINS APPLY TO RIGHT SIDE OF CAGE

△9 PRESS FIT CAGE PINS APPLY TO LEFT SIDE OF CAGE

△10 PRESS FIT OFFSET BETWEEN RIGHT AND LEFT SIDE OF CAGE

△11 DIMENSIONS INCLUDE BACKCOVER

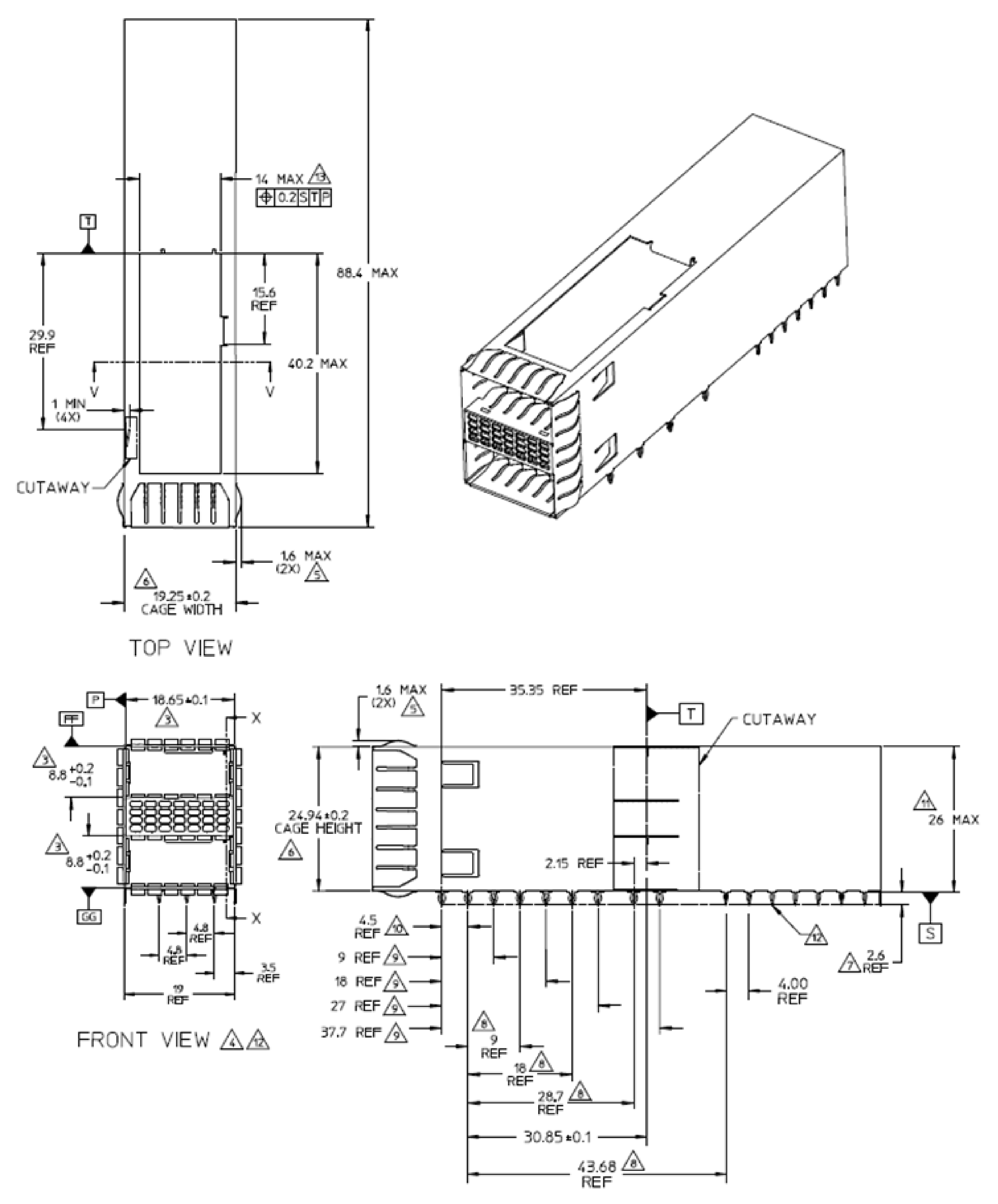
△12 SIZE AND POSITION OF CAGE AND CONNECTOR PRESS FIT PINS SHALL
BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FORMAT FOOTPRINT LAYOUT

△13 CAVITY FOR HEATSINK IS OPTIONAL

△14 CONTACT PIN DIMENSION MEASURED FROM DATUM T.

△15 CONTACT PIN DIMENSION MEASURED FROM DATUM T1.

6



1
2
3 **Figure 48: 2x1 stacked cage**

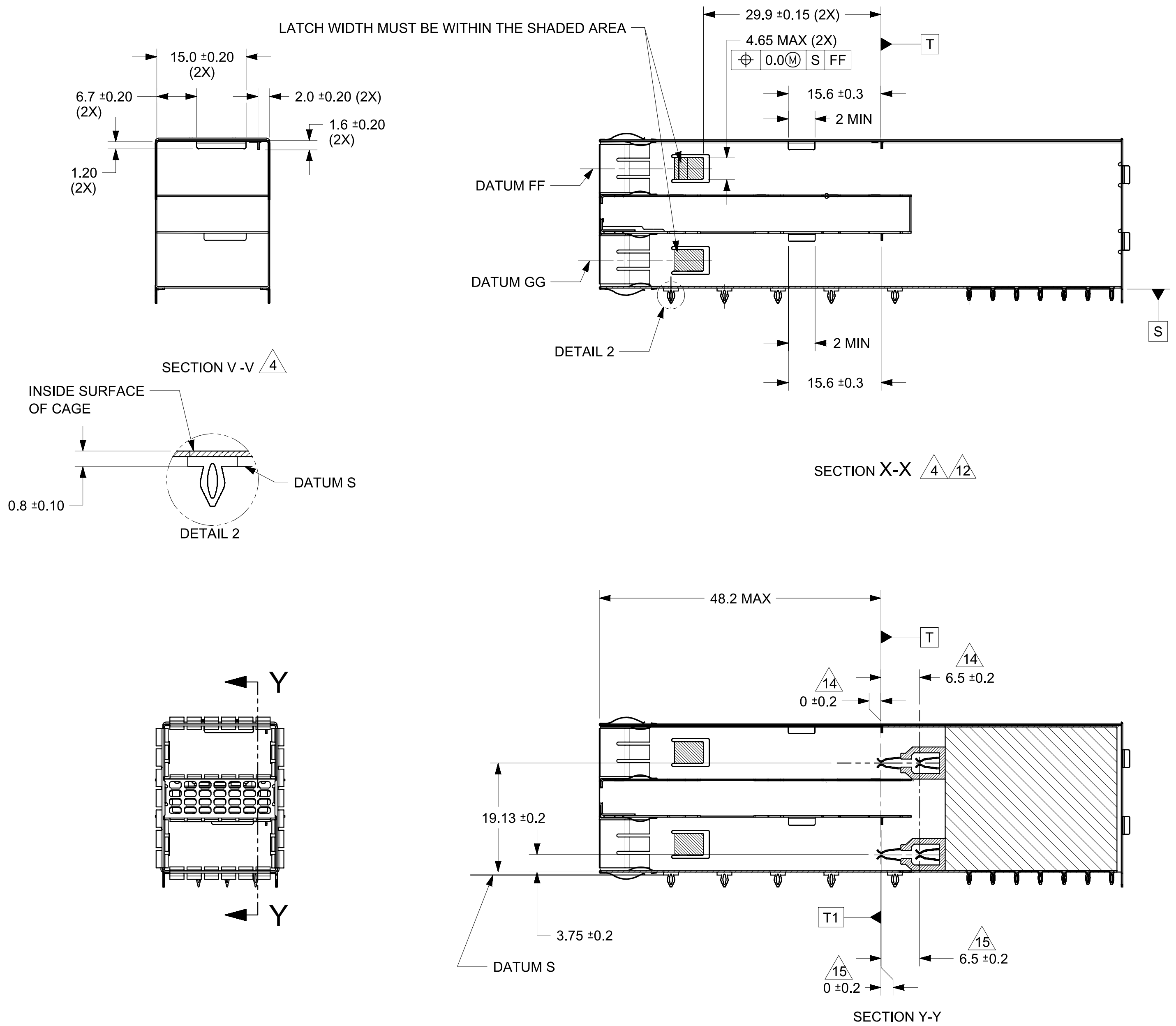


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Figure 49: 2x1 stacked cage dimensions

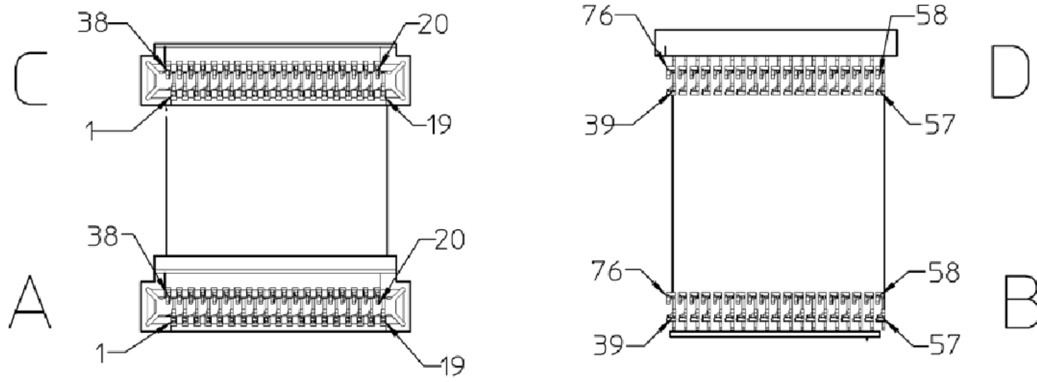
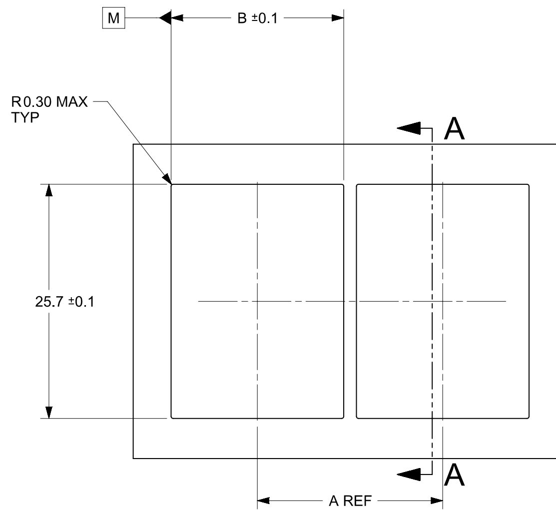


Figure 50: Connector pads in 2x1 stacked cage as viewed from front



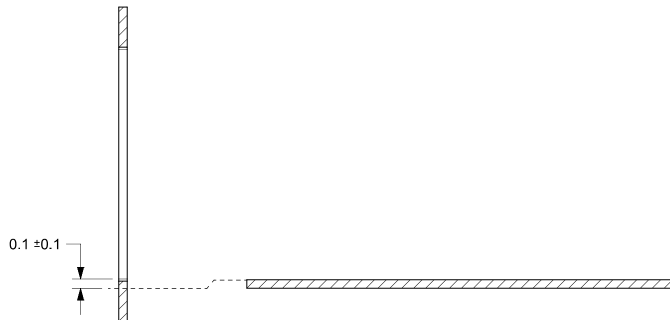


Figure 51: 2x1 Bezel Opening

6.7.1 QSFP-DD 2x1 Connector and Cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD 2x1 Connector and Cage system is shown in Figure 52 and Figure 53. Location of the pattern on the host board is application specific. To achieve 56 Gbps (28 GBd) operation the pad dimensions and associated tolerance must be adhered to and attention paid to the host layout.

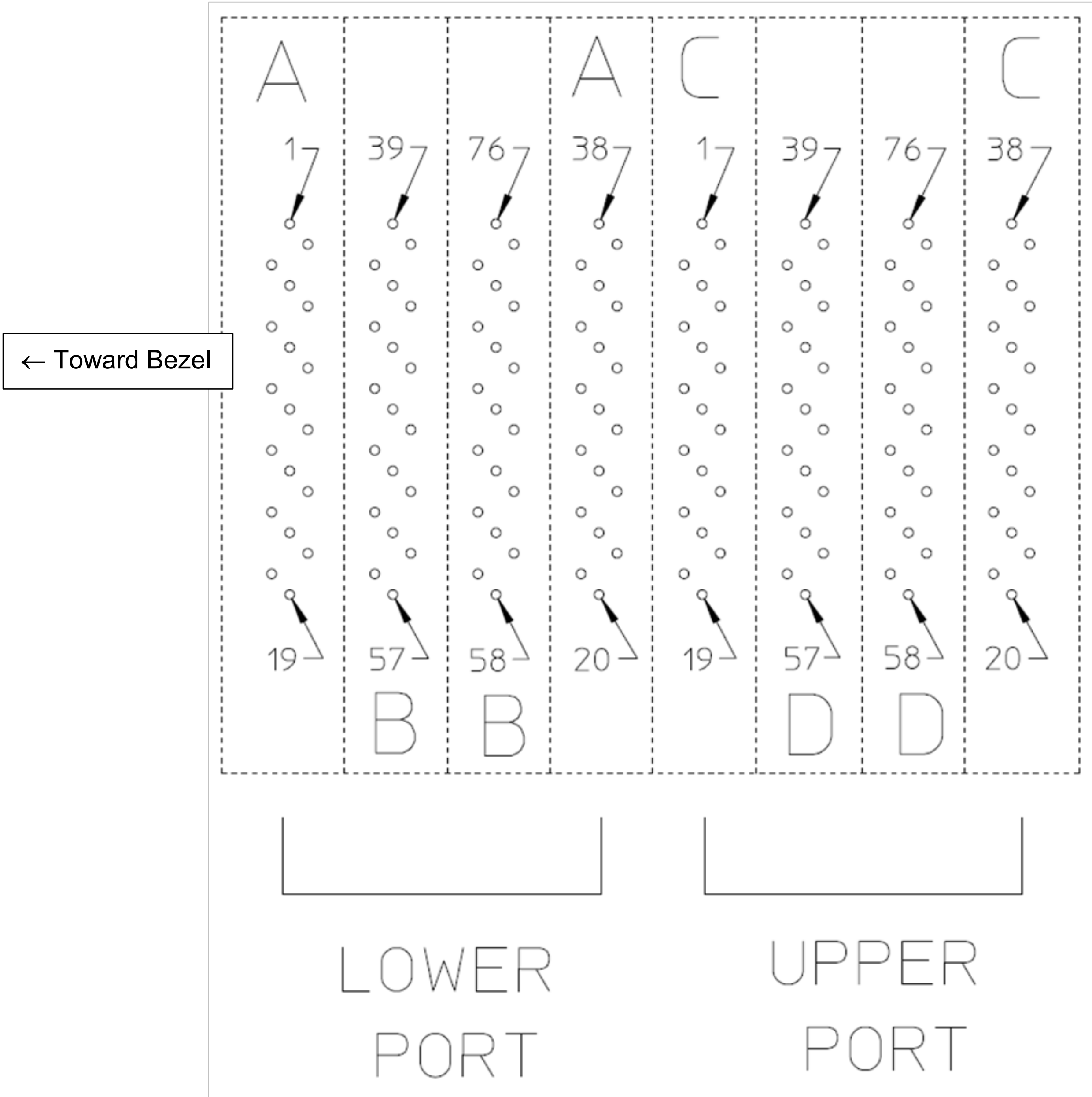
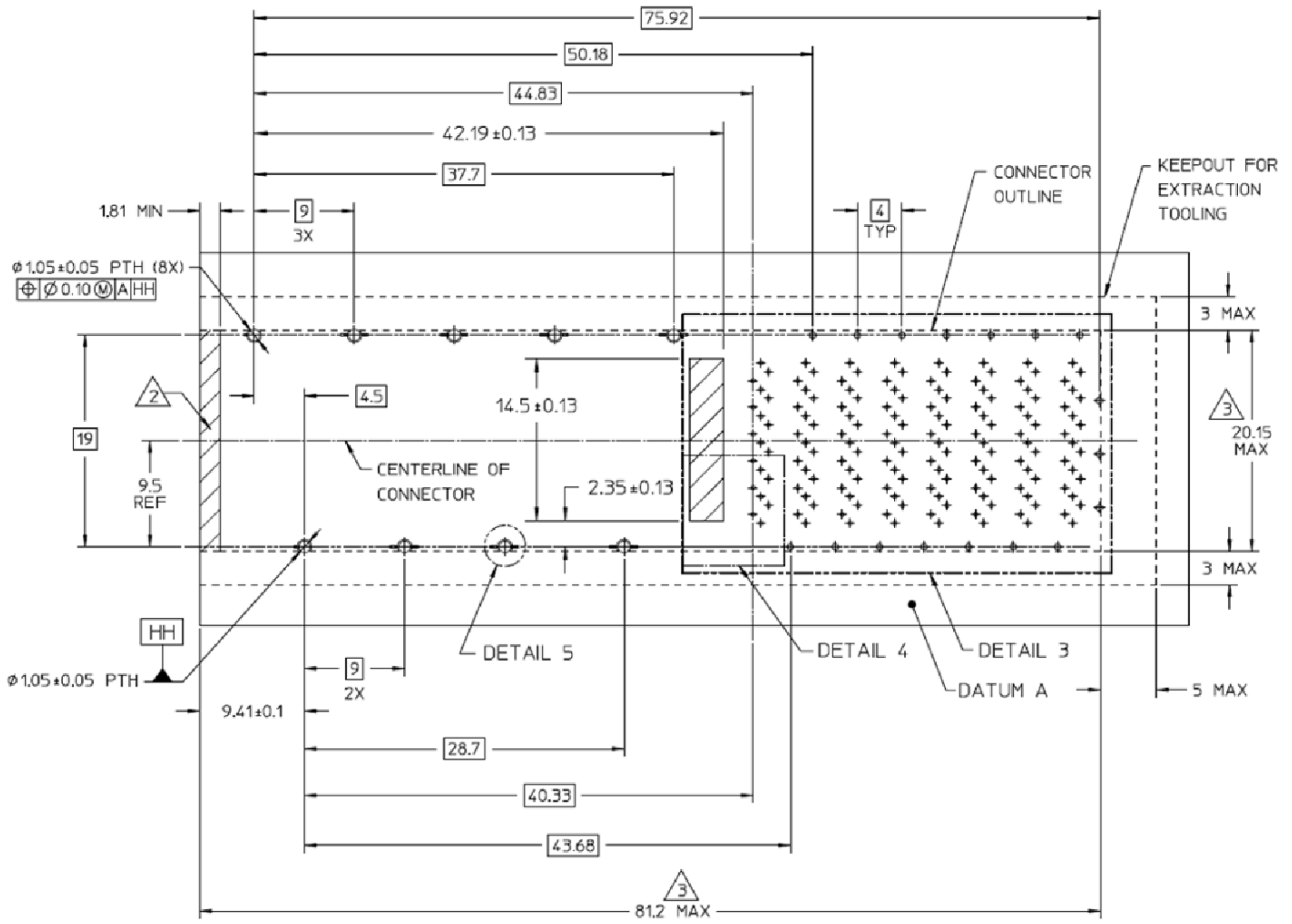


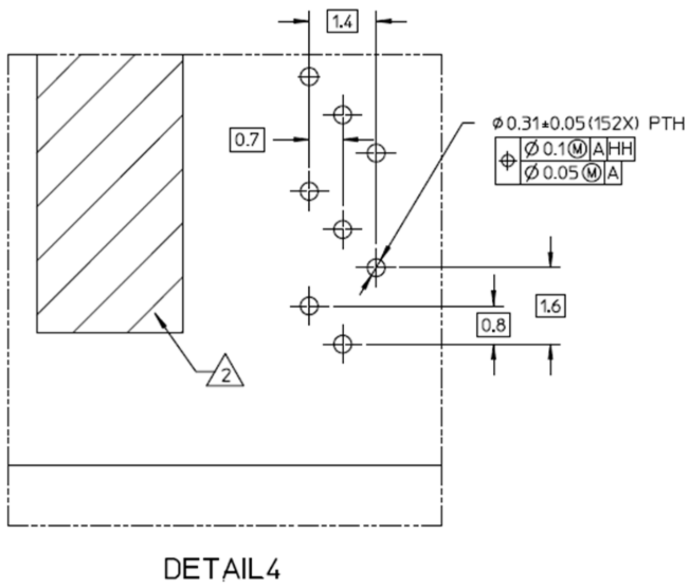
Figure 52: 2X1 host board connector contacts

1



2
3
Figure 53: 2X1 Host PCB layout
4
5

28
4
TYP
2
Ø 0.56±0.05 (17X) PTH
⌖ Ø 0.1Ⓜ A HH
14.4
4.8
19
4.8
3.5
2.18
DATUM HH
3.07±0.13
4
TYP
24
DETAIL 3



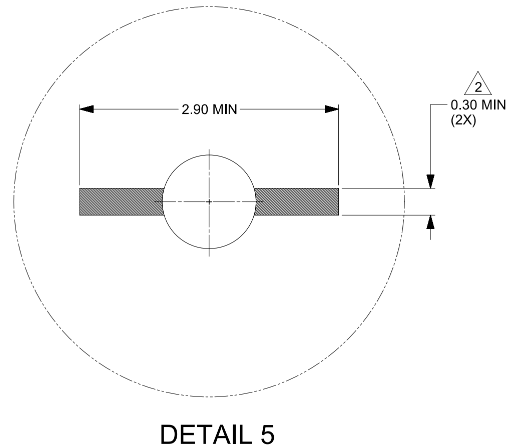


Figure 54: 2X1 Host PCB detail layout

6.8 QSFP-DD Surface Mount Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The SMT connector in a 1xN cage is shown in Figure 55 with detailed drawings in Figure 56 and Figure 57 and Figure 59. SMT connector view and connector detail designs are shown in Figure 58 and Figure 59. Recommendations for the SMT cage bezel opening are shown in Figure 60.

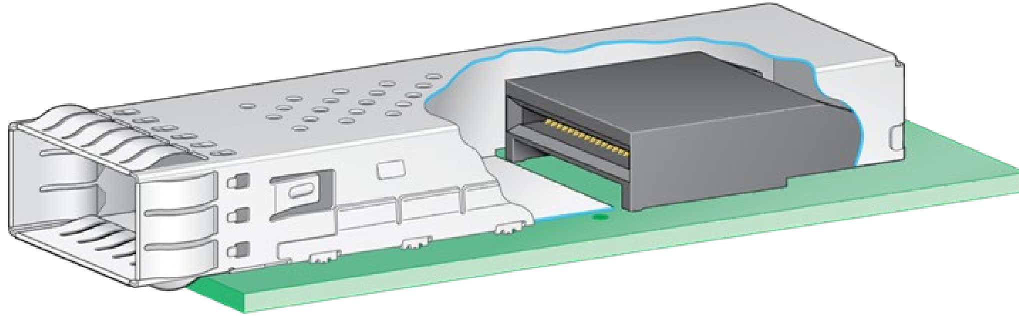


Figure 55: SMT connector in 1xN cage

Notes apply to SMT 1xN cage drawing, see Figure 53, Figure 54, and Figure 55.

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. ALL DIMENSIONS ARE IN MILLIMETERS.

△3 DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED

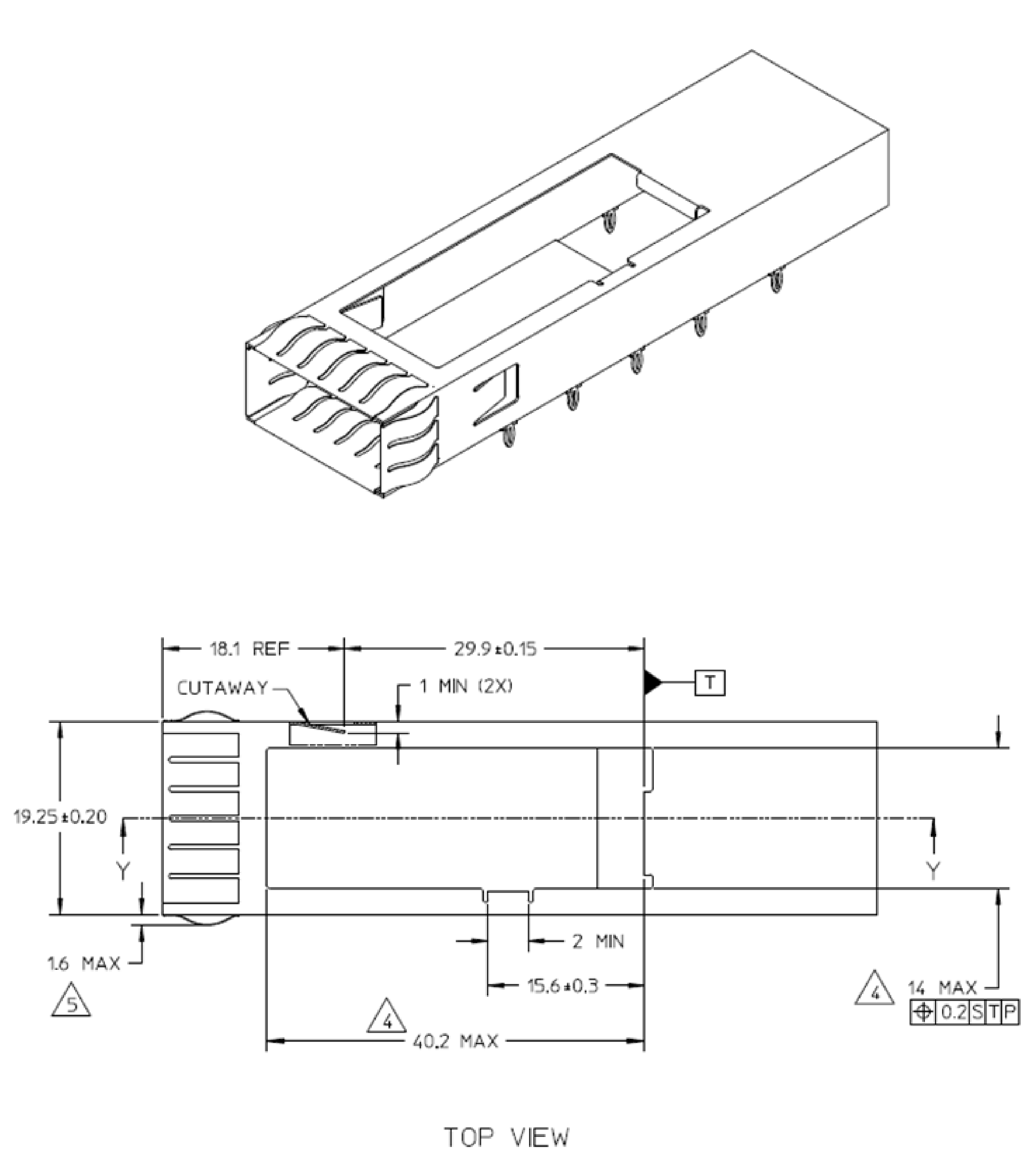
△4 CAVITY FOR HEATSINK IS OPTIONAL

△5 APPLIES TO ALL SPRING FINGERS ON ALL SIDES.

△6 DATUM S IS DEFINED BY SEATING PLANE ON HOST BOARD

△7 SIZE OF CAGE PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT

△8 THIS SURFACE REFERENCES POTENTIAL FEATURES TO SUPPORT MODULES



1
2
3 **Figure 56: SMT 1x1 cage overview**
4

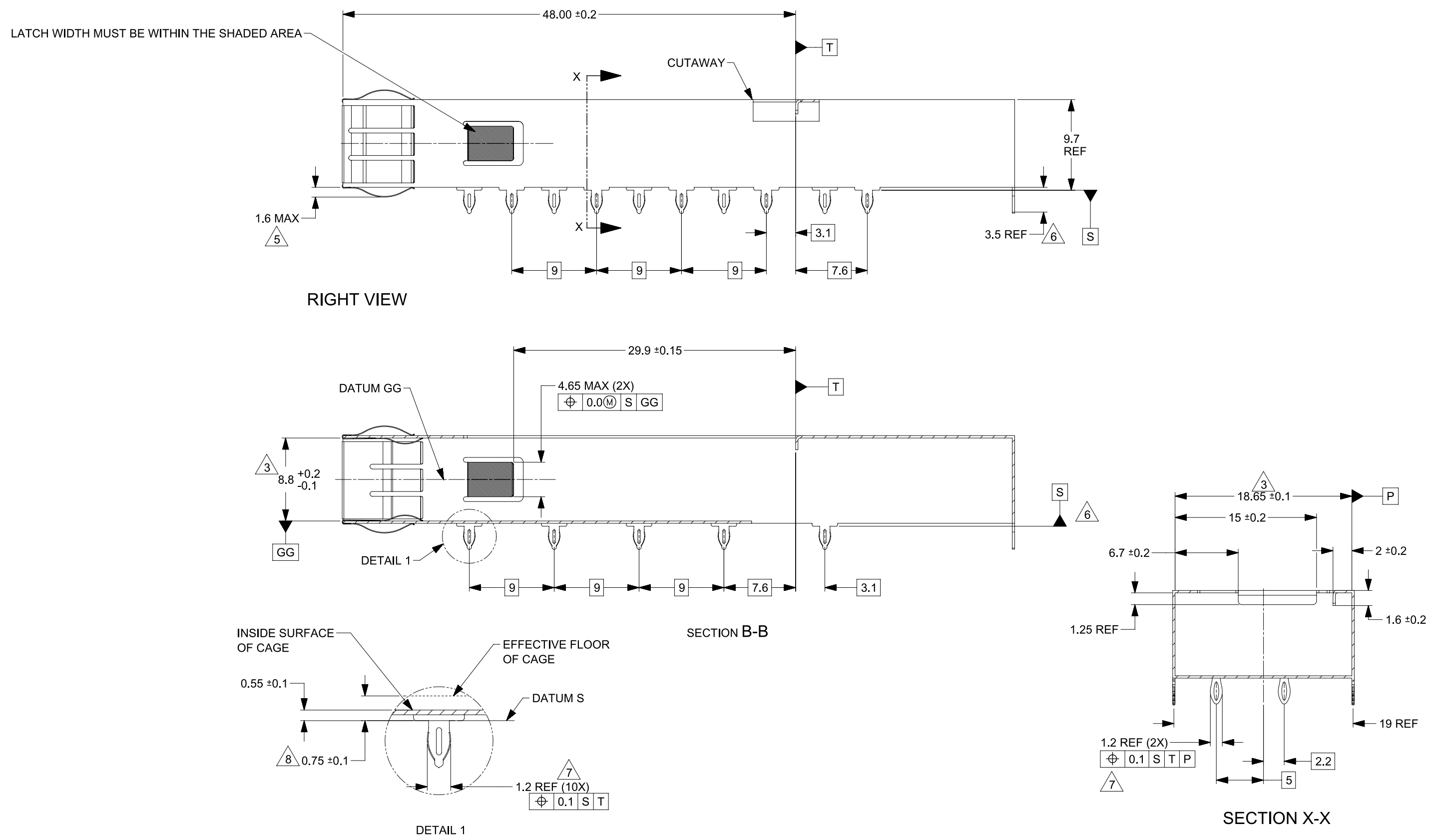


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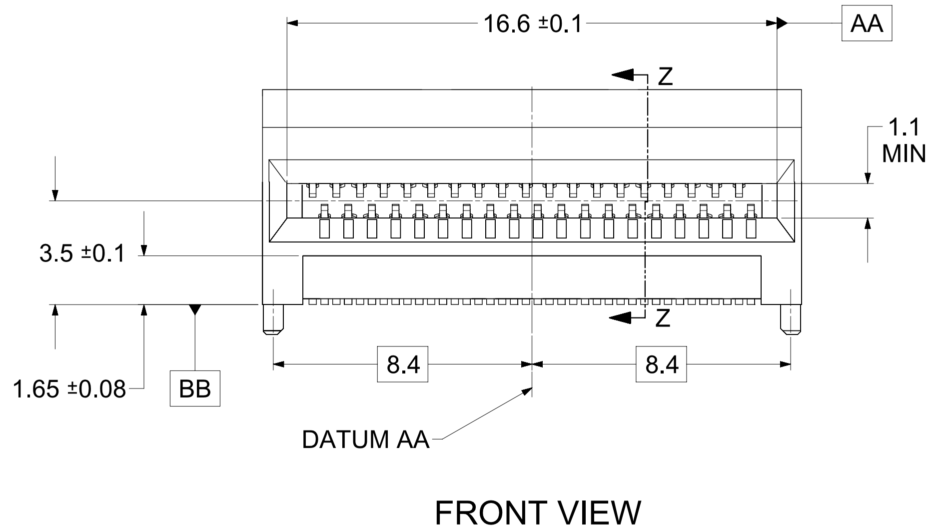
Figure 57: SMT 1x1 cage detail design



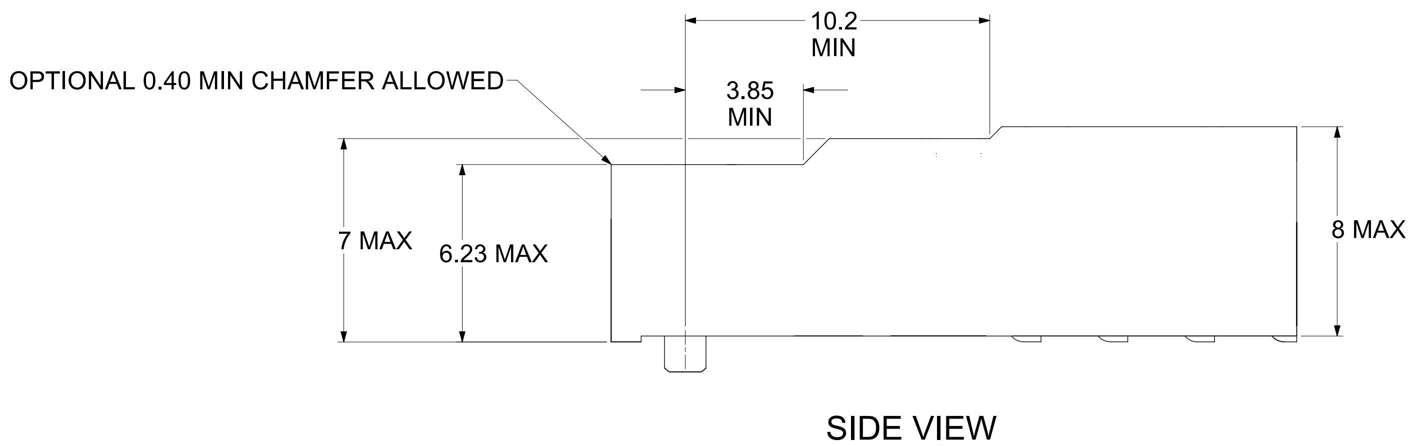
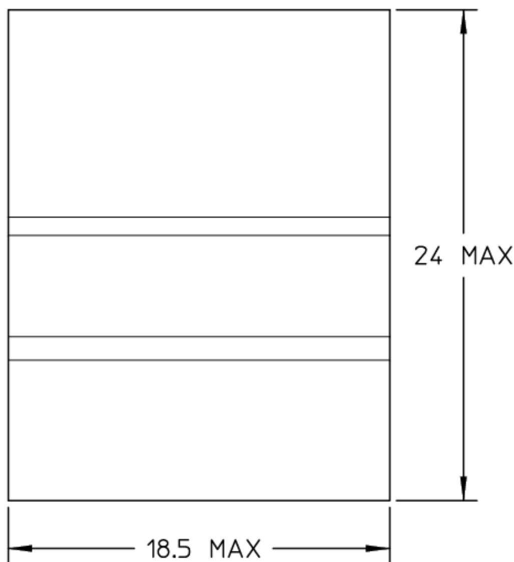
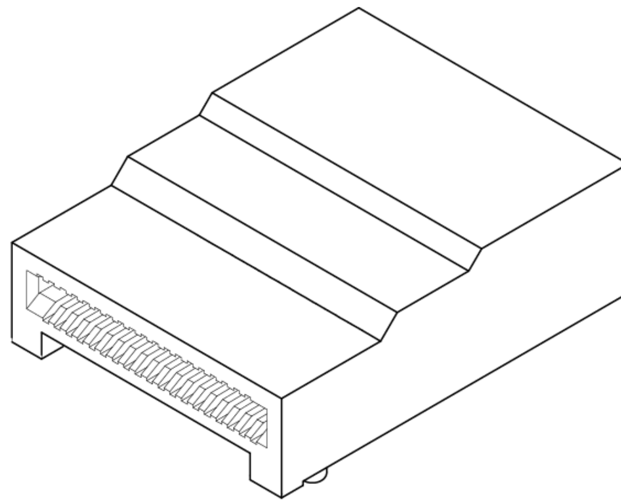
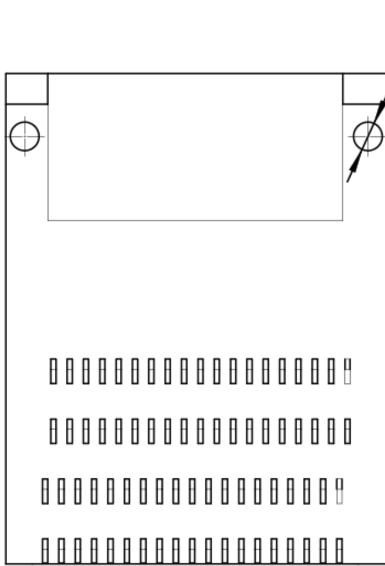


Figure 58: SMT 1x1 connector front and side views







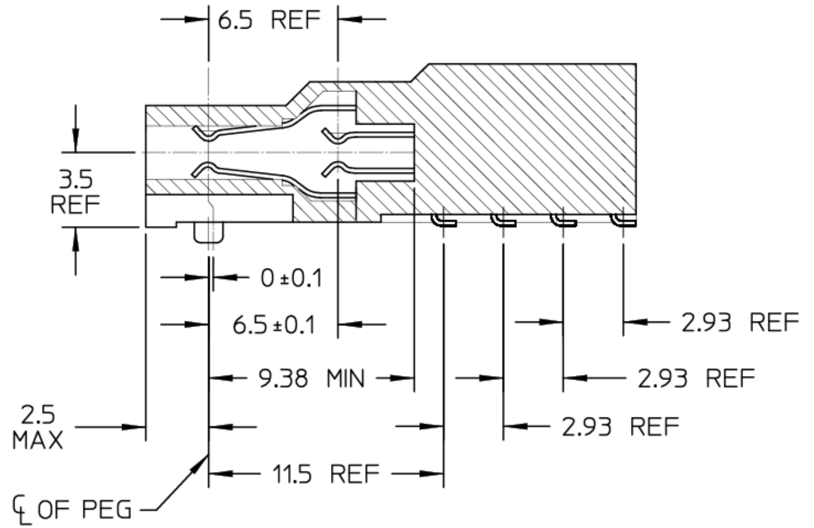
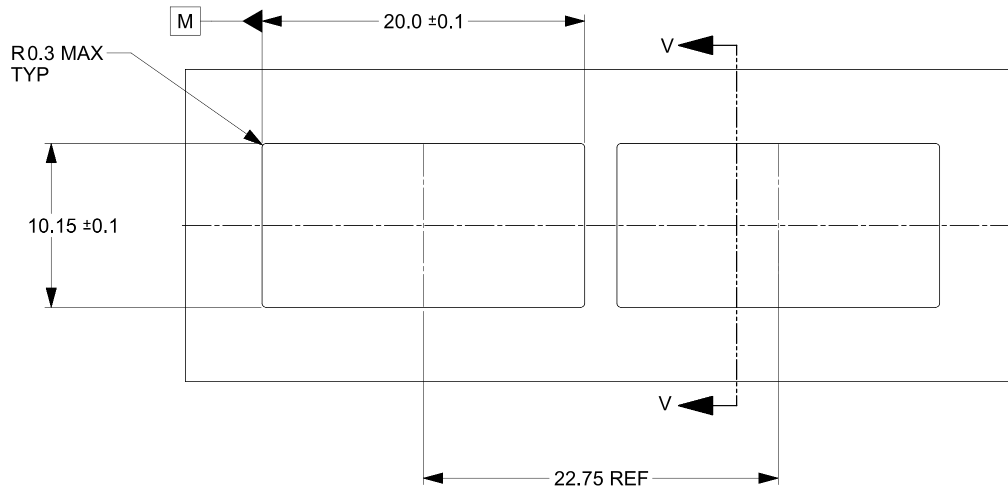


Figure 59: SMT 1x1 connector detail design

Note: Contact Dimension Measured from Datum T



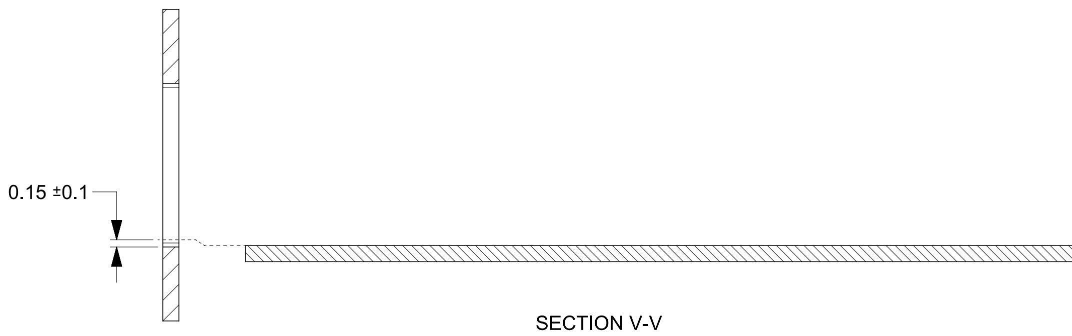


Figure 60: SMT 1x1 bezel opening

6.8.1 QSFP-DD Surface mount connector and cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD surface mount Connector and Cage System is shown in Figure 61 and Figure 62. Location of the pattern on the host board is application specific.

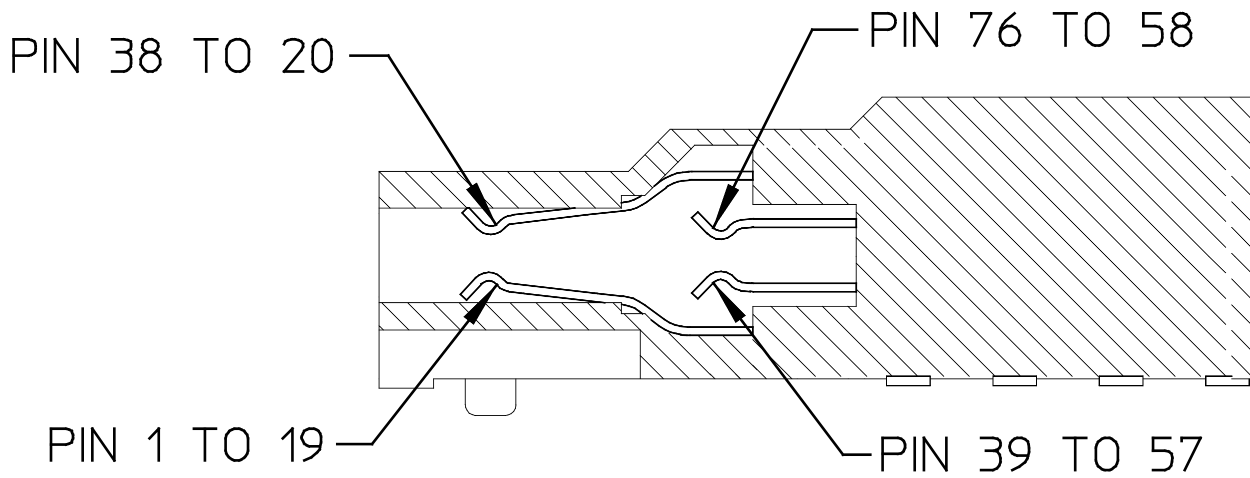
To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

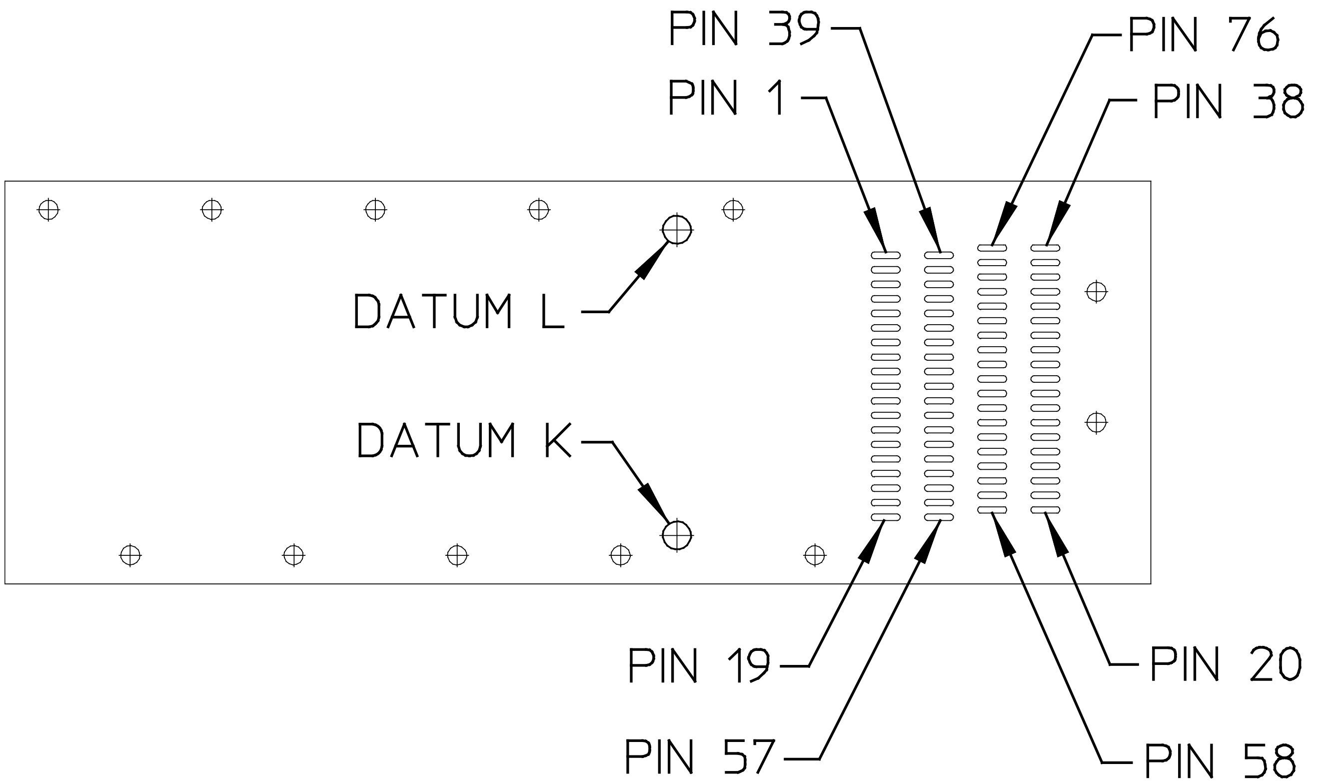
Notes for host PCB requirements (see Figure 61):

1. THE ENTIRE AREA UNDER THE CONDUCTOR (INSIDE DASHED LINES), IS TO BE CONSIDERED A KEEP OUT AREA FOR COMPONENTS.

△2 HATCHED AREAS SHOULD REPRESENT ZONES ON THE PCB THAT COME IN CONTACT WITH OR CLOSE PROXIMITY TO THE PLASTIC HOUSING OR THE CONNECTOR CAGE. INDICATED AREAS TO BE CONSIDERED TRACE FREE.

Figure 61: SMT host PCB layout





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3 **Figure 62: SMT Connector and host PCB contact numbers**
4
5

7 QSFP-DD800 Mechanical and Board Definition

Some of the QSFP-DD800 module mechanical specifications are common with QSFP-DD, below are the list of relevant sections applicable to QSFP-DD800/QSFP-DD1600:

- 6.1 Introduction to QSFP-DD/QSFP-DD800/QSFP-DD1600 Modules
- 6.2 Datums, Dimensions and Component Alignment
- 6.3 Module Form Factors for QSFP-DD/QSFP-DD800/QSFP-DD1600
- 6.4 Module Flatness and Roughness
- 6.6 Module Extraction and Retention Forces.

7.1 Introduction

The module paddle card dimensions of the QSFP-DD800 have been improved to support 112 Gb/s PAM4 (up to 56 GBd) serial data rates, see Section 7.3.

QSFP-DD800 supports multiple connector/cage form factors. QSFP-DD800 cages/connectors/modules are compatible with QSFP-DD cages/connectors/modules, QSFP-DD cages/connectors also accepts QSFP family of modules. Examples of QSFP-DD800 cages are:

- 1x1 surface mount connector/cage
- 2x1 surface mount connector/cage
- 2x1 surface mount connector/cage with cabled high-speed host interconnects on the top connector/ upper port of the cage.

7.2 QSFP-DD800 module mechanical dimensions

For QSFP-DD800 modules the bottom surface of the module within the cage shall be flat without a pocket. The options for the position of the label could include the bottom surface of the module that protrudes outside the bezel of the cage or etched into the metal surface. Caution should be exercised that any etchings do not affect thermal performance. Flatness and roughness specs as defined in 6.4 apply for both top and bottom surfaces of QSFP-DD800 module, see Figure 63 and Figure 64.

NOTES APPLY TO MODULE DRAWING

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. UNLESS OTHERWISE SPECIFIED, SHARP CORNERS, EDGES, AND BURRS ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS TO A MINIMUM RADIUS OF 0.20 MM.

4. DIMENSION DEFINES ENLARGED SECTION OF TRANSCEIVER THAT EXTENDS OUTSIDE OF CAGE TO ACCOMMODATE MATING PLUG AND ACTUATOR MECHANISM.

5. SURFACES ON ALL 4 SIDES OF THE 12.4 MIN DIMENSION TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

6. DIMENSION APPLIES TO LATCH MECHANISM.

7. DIMENSION APPLIES TO THE LOCATION OF THE EDGE OF THE MODULE BOARD PAD, DATUM H, CONTACTS 21, 22, 36 AND 37 ARE VISIBLE.

8. DIMENSION TO INCLUDE BAIL TRAVEL.

9. DIMENSION APPLY TO OPENINGS IN THE HOUSING.

10. OPTIONAL FEATURE TO AID INSPECTION OF DIMENSIONS FROM DATUM D.

11. FLATNESS AND SURFACE ROUGHNESS (Ra) APPLIES FOR INDICATED LENGTH AND MIN WIDTH OF 13MM. SURFACE TO BE THERMALLY CONDUCTIVE. SEE SECTION 6.4, TABLE 17 AND TABLE 18 FOR FLATNESS AND ROUGHNESS REQUIREMENTS.

12. HIGHER WATTAGE MODULES MAY REQUIRE ADDITONAL SPACE FOR COOLING.

13. BLOCKING FEATURE IS CRITICAL TO APPLICATION FUNCTION. A RADIUS OF 0.2 ± 0.05 MM IS REQUIRED ON THE LEADING EDGES OF THIS FEATURE.

14. NO LABEL SHALL BE APPLIED IN THIS AREA. ETCHINGS ARE ALLOWED BUT MUST NOT AFFECT THERMAL PERFORMANCE.

15. THE LABEL(S) MUST NOT INTERFERE WITH THE MECHANICAL, THERMAL, OR EMI PERFORMANCE AND MUST NOT VIOLATE NOTE 5.

16. DIMENSION APPLIES TO LATCH POCKET.

17. OPTIONAL FEATURE TO AID IN TOOLING STRENGTH

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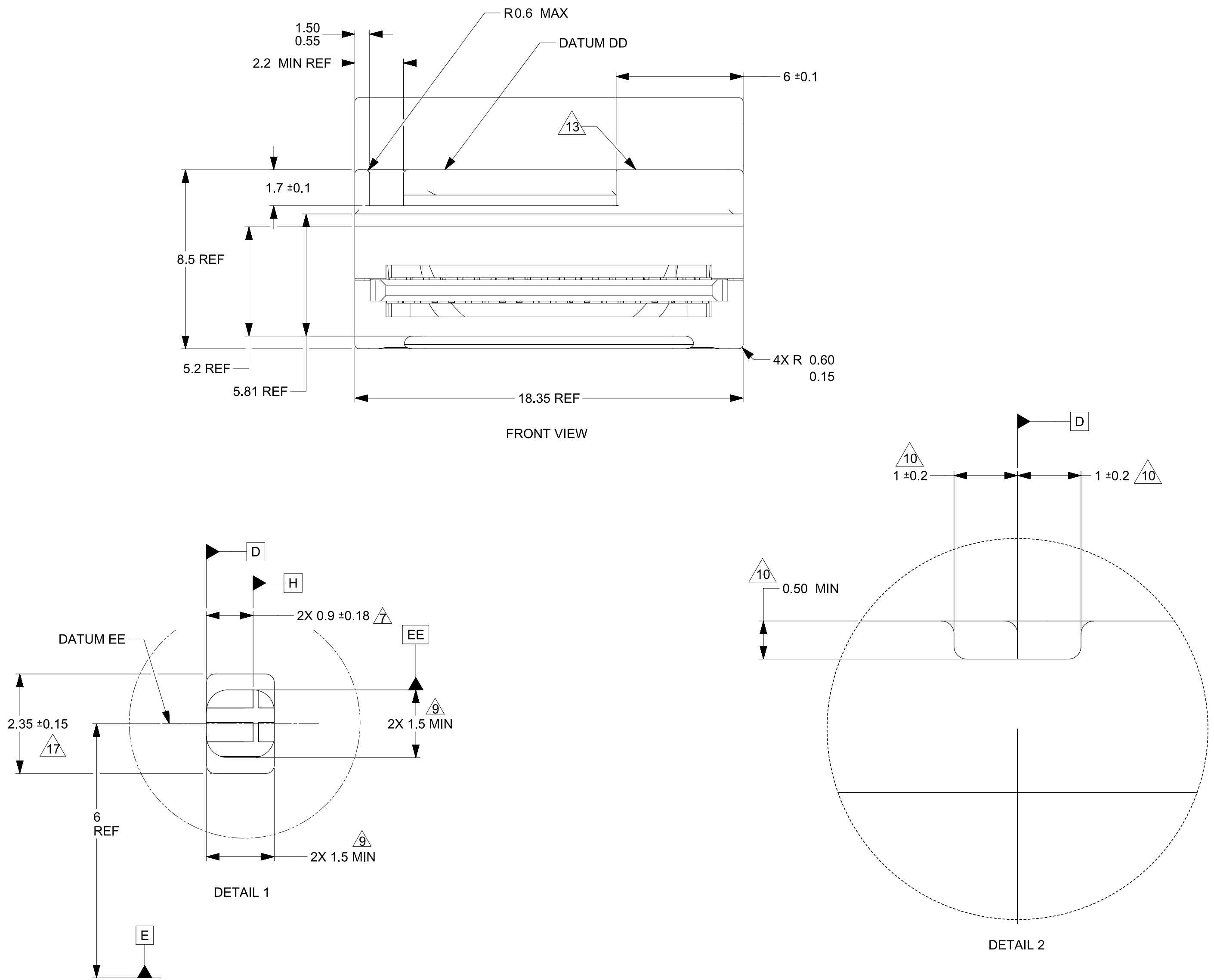
Figure 63: QSFP-DD800 module dimensions



1
2
3 **Figure 64: QSFP-DD800 module leading edge dimensions**
4

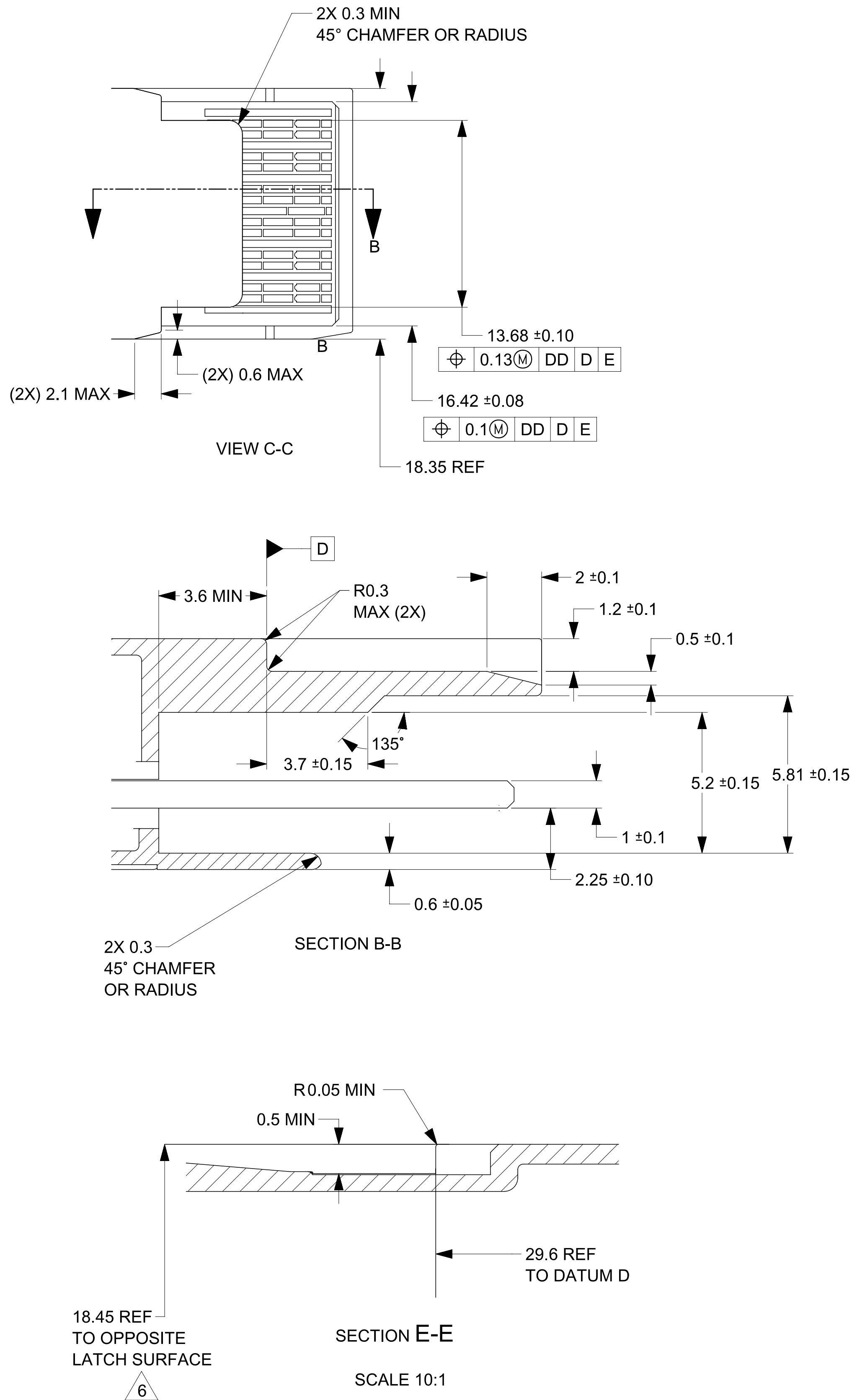


Figure 65: Detailed dimensions of the module opening

1
7.3 QSFP-DD800 improved module paddle card dimensions

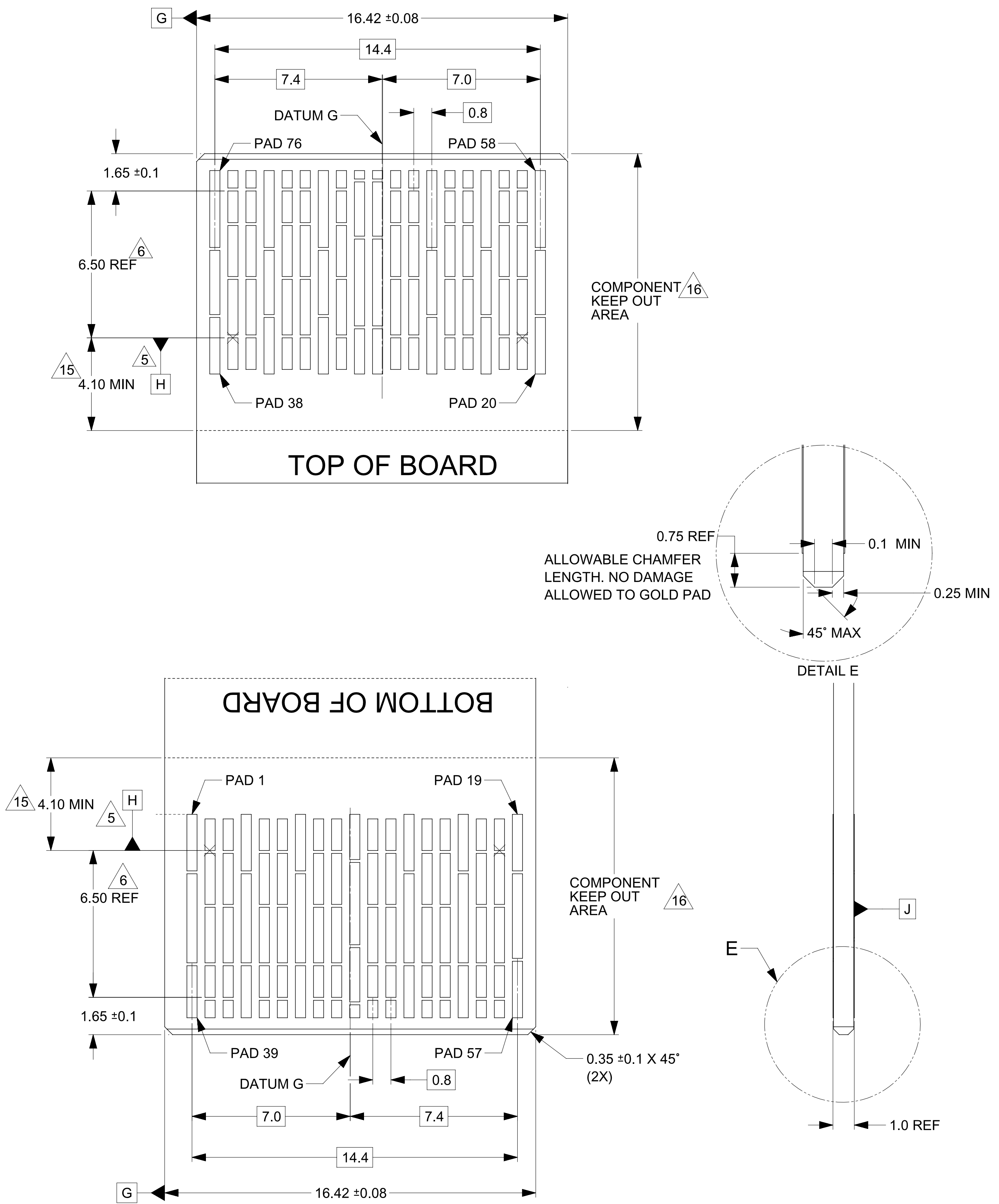
2 The QSFP-DD800 module paddle card pad dimensions have been modified to support 112 Gb/s PAM4 (56
3 GBd) serial data rates. See Figure 66 and Figure 67 for QSFP-DD800 module updated paddle card pad
4 dimensions. All other module dimensions, except for the pads, remain the same as the QSFP-DD Hardware
5 Specification defined in Chapter 6.
6

NOTES APPLY TO MODULE PADDLE CARD:

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD
5. (△) DATUM H IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTERMOST SIGNAL CONTACT PADS TO BE RE-ESTABLISHED ON EACH SIDE
6. (△) DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS
7. (△) DIMENSION AND TOLERANCE APPLIES TO ALL GROUND PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
8. (△) DIMENSION AND TOLERANCE APPLIES TO ALL POWER PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
9. (△) DIMENSION AND TOLERANCE APPLIES TO ALL SIGNAL PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
10. (△) A ZERO GAP IS ALLOWED FOR A CONTINIOUS SIGNAL PADS ON BOTH TOP AND BOTTOM
11. (△) APPLIES TO ALL SIGNAL PAD TO PRE-WIPE SPACING
12. (△) PRE-WIPE PADS (SHADED AREA), ON MODULE CARD HOST ARE OPTIONAL
13. (△) PRE-WIPE PADS (UNSHADED AREA), ARE REQUIRED EXCEPT IN CONTINUOUS POWER AND GROUND DESIGNS
14. (△) PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS MUST NOT BE PROUD OF THE PAD SURFACE
15. (△) MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS
16. (△) COMPONENT KEEP OUT AREA MUST MEASURE FROM DATUM H
17. (△) A SINGLE, DOUBLE AND TRIPLE SPLIT IN THE PRE-WIPE SIGNAL PAD IS OPTIONAL. AND IF IMPLEMENTED THE RESULTING 2, 3, AND 4 PADS SHALL BE SEPARATED WITH A GAP OF 0.13+/- 0.05
18. (△) CONTACT PAD PLATING
    - 0.38 MICROMETERS MINIMUM GOLD OVER
    - 1.27 MICROMETERS MINIMUM NICKEL

    ALTERNATE CONTACT PAD PLATING
    - 0.05 MICROMETERS MINIMUM GOLD OVER
    - 0.30 MICROMETERS MINIMUM PALLADIUM OVER
    - 1.27 MICROMETERS MINIMUM NICKEL

7



1
2
3 **Figure 66: QSFP-DD800 Module paddle card dimensions**
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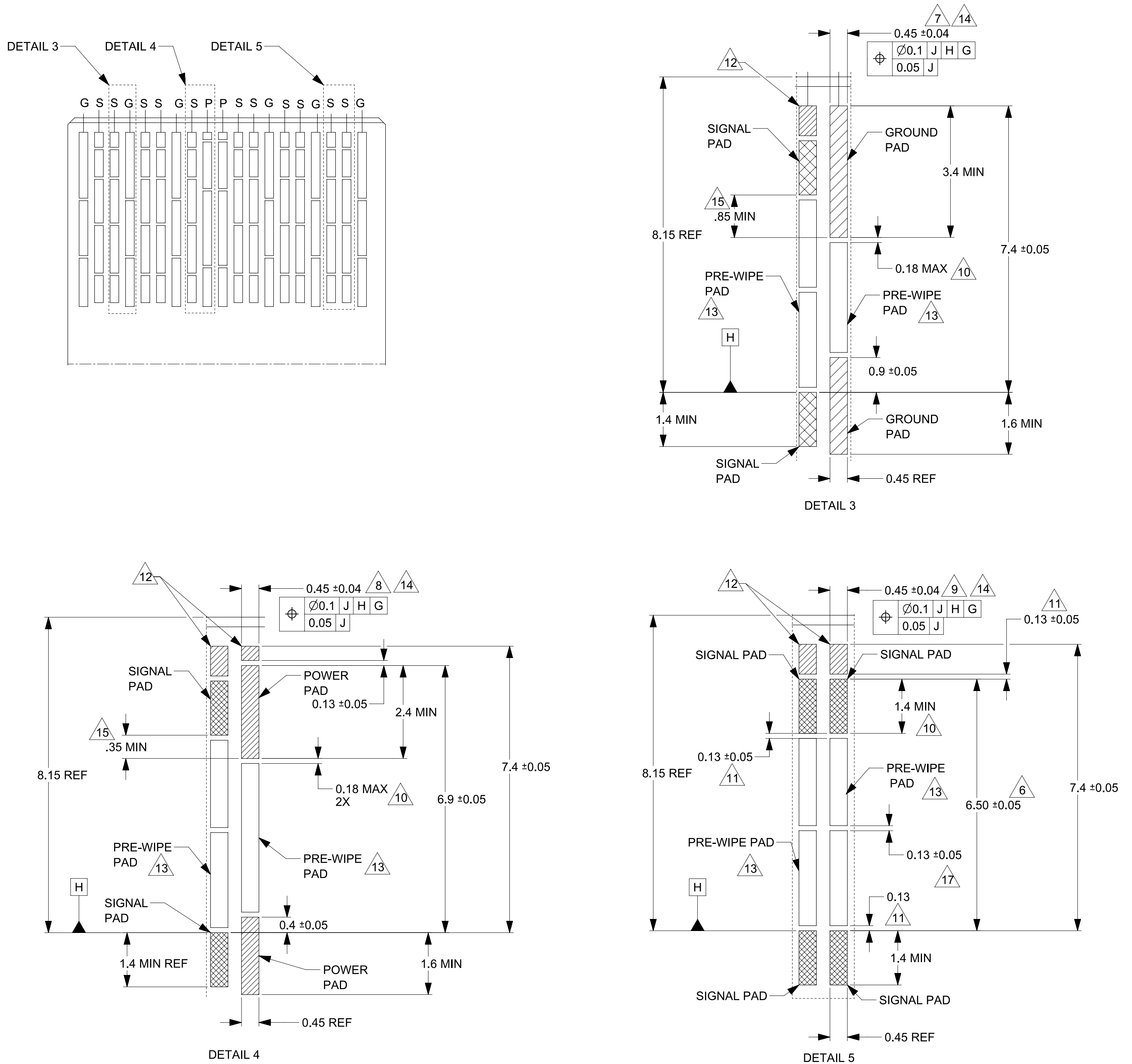
5



1
2 **Figure 67: QSFP-DD800 detail module paddle card dimensions**
3

7.4 QSFP-DD800 1x1 SMT connector/cage

The 1x1 SMT connector/cage mechanical outline for QSFP-DD800 is the same as the QSFP-DD 1x1 connector/cage, see 6.8.

7.4.1 Surface mount connector and cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD surface mount Connector and Cage System is shown in Figure 68. Location of the pattern on the host board is application specific.

To achieve 112 Gbps (56 GBd) operation the QSFP-DD800 pad dimensions and associated tolerances have improved compared to QSFP-DD and one must adhere and pay attention to the host board layout.

Notes for host PCB requirements (see Figure 68):

1. THE ENTIRE AREA UNDER THE CONDUCTOR (INSIDE DASHED LINES), IS TO BE CONSIDERED A KEEP OUT AREA FOR COMPONENTS.

2 (in triangle) HATCHED AREAS SHOULD REPRESENT ZONES ON THE PCB THAT COME IN CONTACT WITH OR CLOSE PROXIMITY TO THE PLASTIC HOUSING OR THE CONNECTOR CAGE. INDICATED AREAS TO BE CONSIDERED TRACE FREE.

Figure 68: Reduced pad SMT host PCB layout

7.5 2x1 Surface Mount Technology (SMT) Connector/Cage

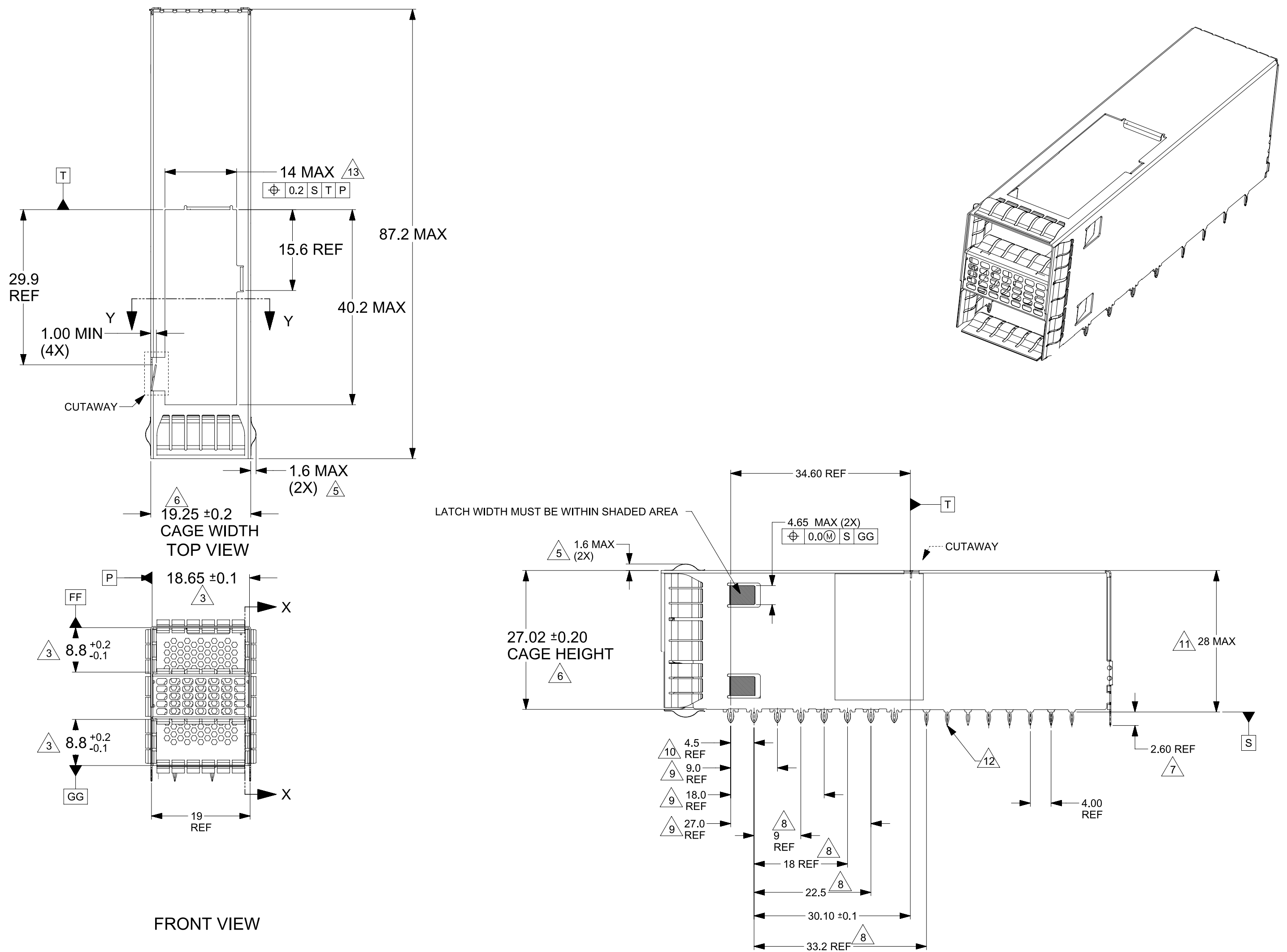
The QSFP-DD800 2x1 SMT connector/cage mechanical outline has similar dimensions as the QSFP-DD 2x1 press fit connector/cage, see 6.7.

7.5.1 2x1 SMT Connector/Cage System

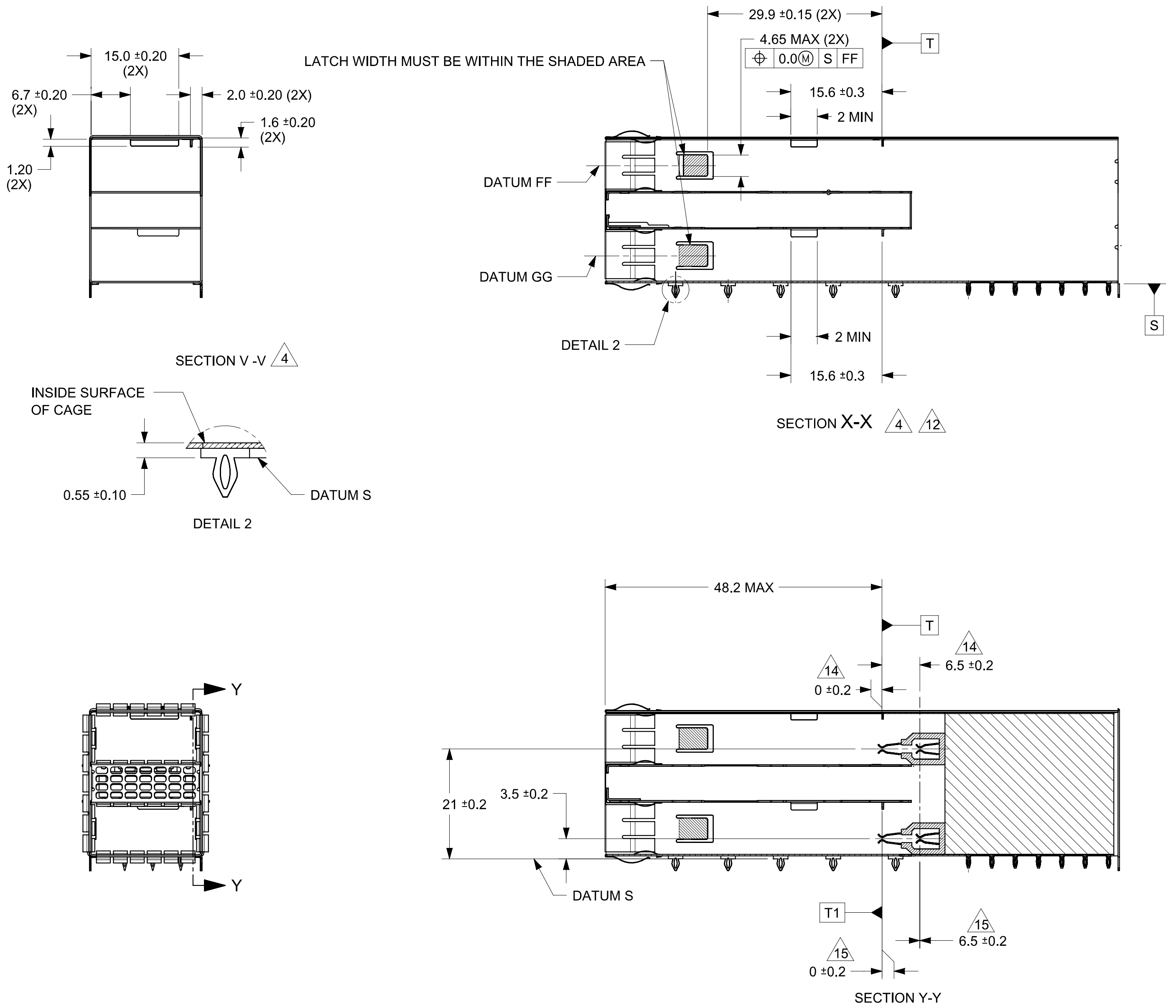
Each of the QSFP-DD800 stacked connectors are a 76-contacts right angle connector. A typical host board mechanical layout for attaching the QSFP-DD800 surface mount connector and cage system are shown in Figure 69 and Figure 70. QSFP-DD800 2x1 connector pad assignment view and bezel opening are shown in Figure 71 and Figure 72. SMT pad labeling shown in Figure 73. Location of the pattern on the host board is application specific.

To achieve 112 Gbps (56 GBd) operation the QSFP-DD800 pad dimensions and associated tolerances have improved compared to QSFP-DD and one must adhere and pay attention to the host board layout.

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED
4. CONNECTOR REMOVED FOR CLARITY
5. APPLIES TO ALL SPRING FINGERS ON ALL SIDES
6. EXTERNAL CAGE DIMENSIONS DOES, NOT INCLUDE FOLDING TABS
7. LENGTH OF CAGE AND SIGNAL TAILS
8. PRESS FIT CAGE PINS APPLY TO RIGHT SIDE OF CAGE
9. PRESS FIT CAGE PINS APPLY TO LEFT SIDE OF CAGE
10. PRESS FIT OFFSET BETWEEN RIGHT AND LEFT SIDE OF CAGE
11. DIMENSIONS INCLUDE BACKCOVER
12. SIZE AND POSITION OF CAGE AND CONNECTOR PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FORMAT FOOTPRINT LAYOUT
13. CAVITY FOR HEATSINK IS OPTIONAL
14. CONTACT PIN DIMENSION MEASURED FROM DATUM T.
15. CONTACT PIN DIMENSION MEASURED FROM DATUM T1.



1
2
3 **Figure 69: QSFP-DD800 2x1 SMT Stack Cage**



1
2
3 **Figure 70: QSFP-DD800 2x1 SMT cage dimensions**
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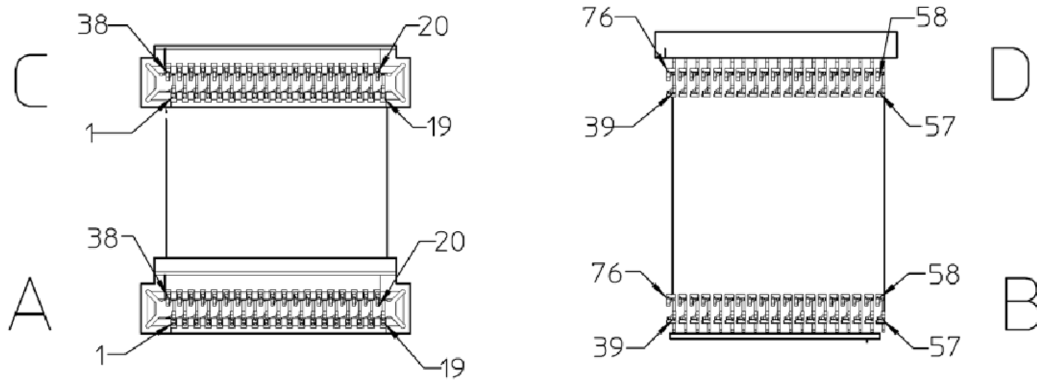

2
3 **Figure 71: Connector pads in 2x1 SMT stacked cage as viewed from front**
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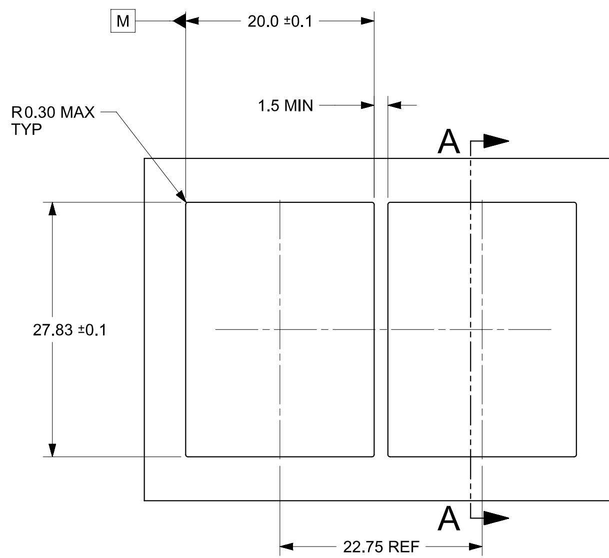

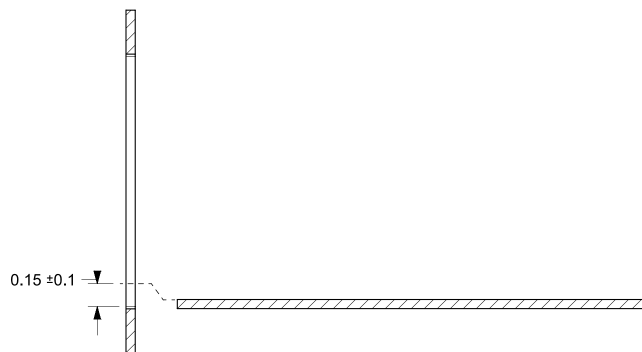

6
7 **Figure 72: QSFP-DD800 2x1 SMT Bezel Opening**

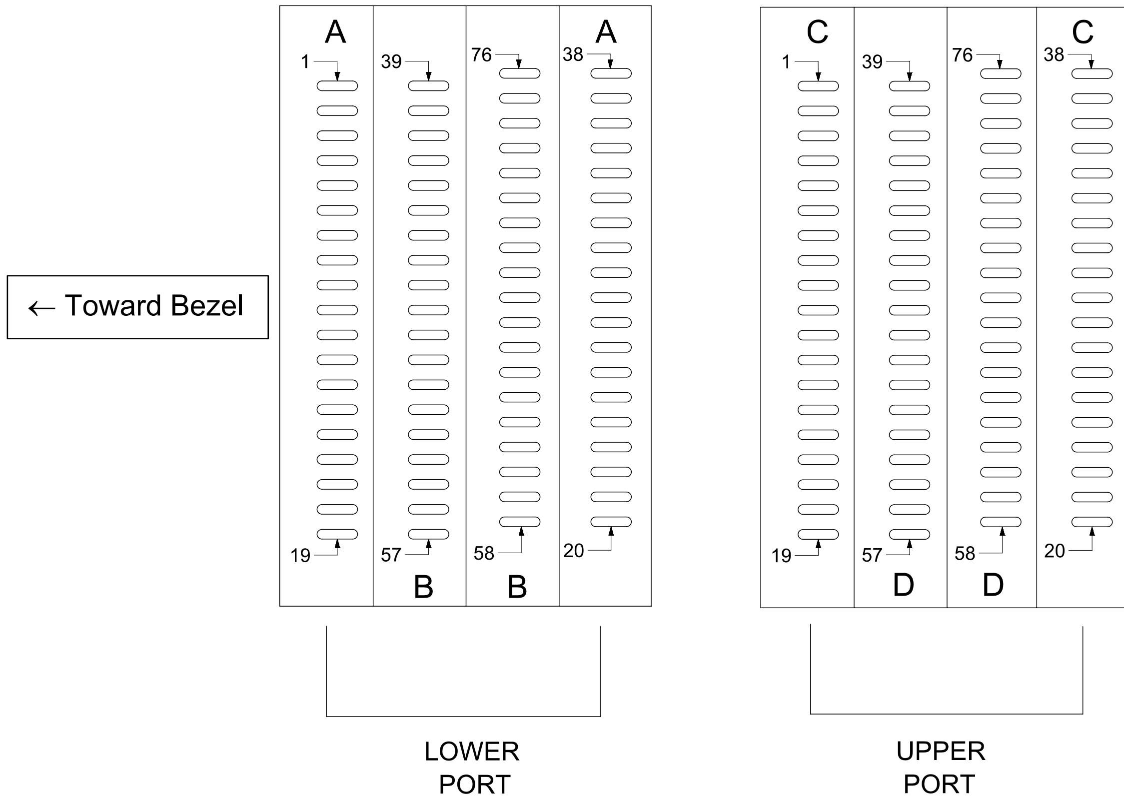

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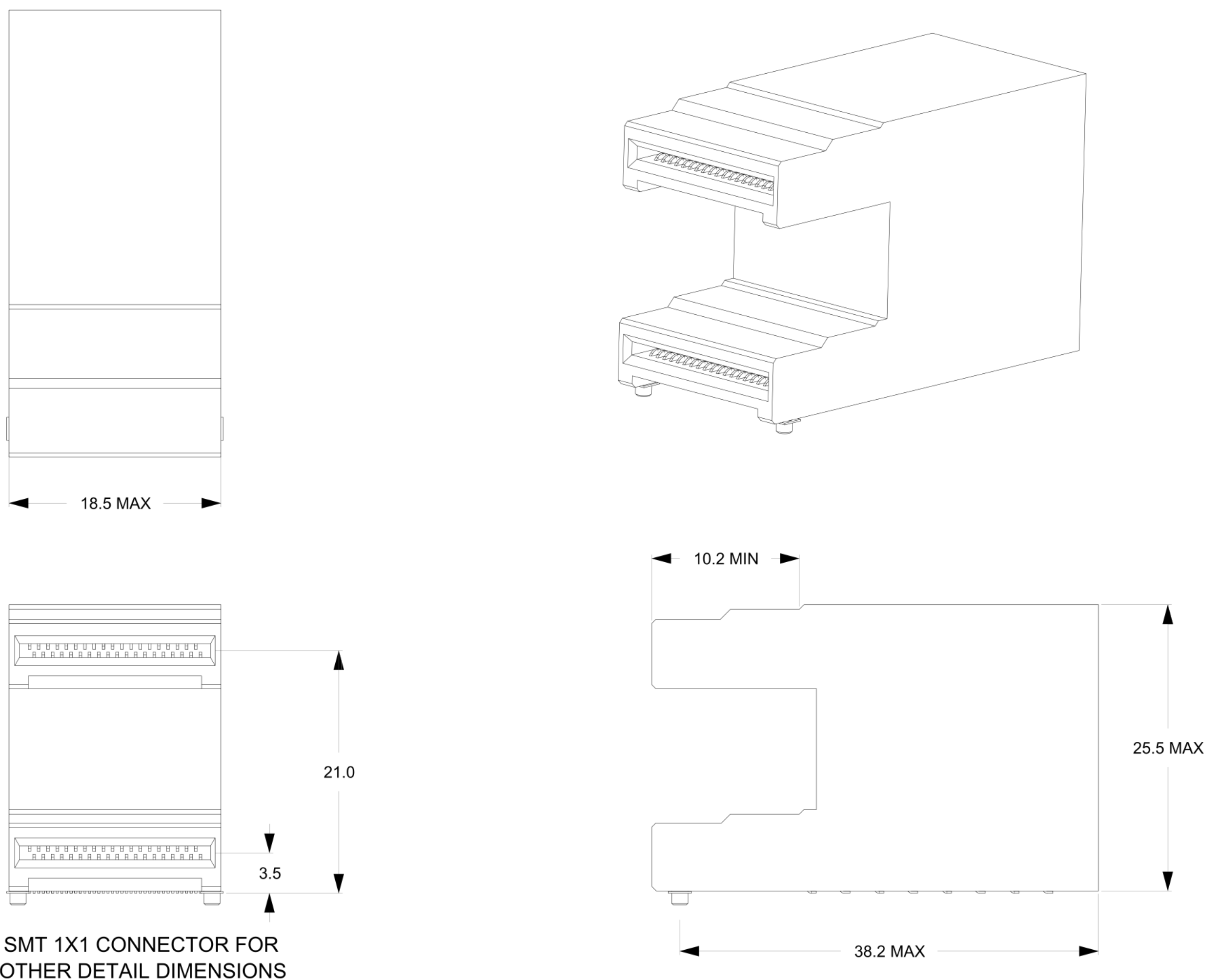
Figure 73: 2x1 SMT Pads Labeling

1 **7.5.2 2x1 SMT Connector and Cage host PCB layout**

2 QSFP-DD800 2x1 connector and cage system shown in Figure 74, details dimensions not shown are identical
3 to QSFP-DD 1x1 SMT connector Figure 58. The QSFP-DD800 2x1 connector and cage host PCB
4 implementations with solder ring shown in Figure 75 and with press fit shown in Figure 76. Examples of host
5 board layout implementations for attaching the.

6 The detail host PCB layout for QSFP-DD800 is shown in Figure 77. Location of the pattern on the host board
7 is application specific. To achieve 112 Gbps (56 GBd) operation pad dimensions and associated tolerance
8 must be adhered to, and attention paid to the host layout.

9



10

11 **Figure 74: QSFP-DD800 stacked SMT 2x1 connector**

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13

Notes for host PCB requirements (see Figure 75, Figure 76, and Figure 77):

1. THE ENTIRE AREA UNDER THE CONDUCTOR (INSIDE DASHED LINES), IS TO BE CONSIDERED A KEEP OUT AREA FOR COMPONENTS.

2 (in a triangle) HATCHED AREAS SHOULD REPRESENT ZONES ON THE PCB THAT COME IN CONTACT WITH OR CLOSE PROXIMITY TO THE PLASTIC HOUSING OR THE CONNECTOR CAGE. INDICATED AREAS TO BE CONSIDERED TRACE FREE.

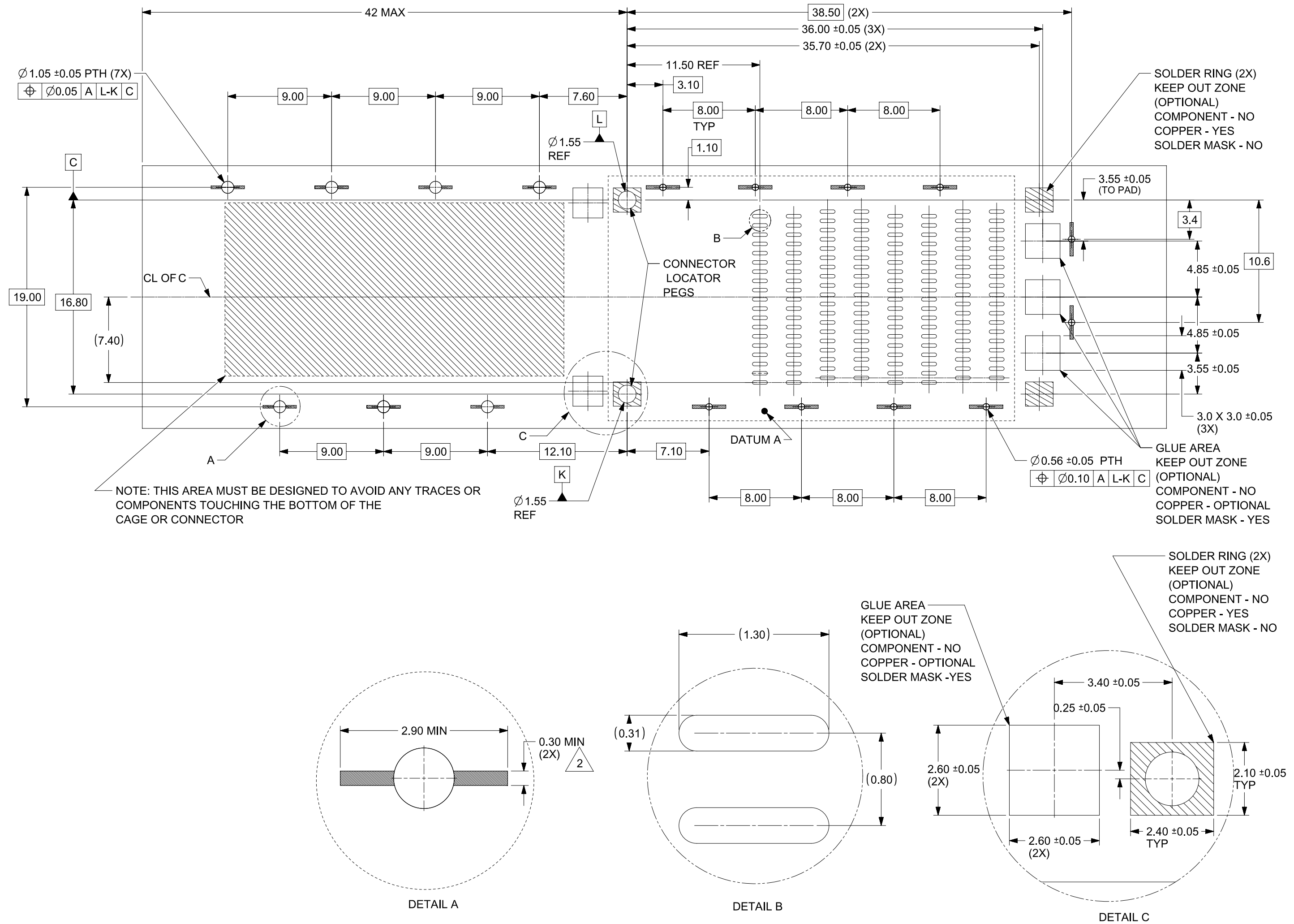
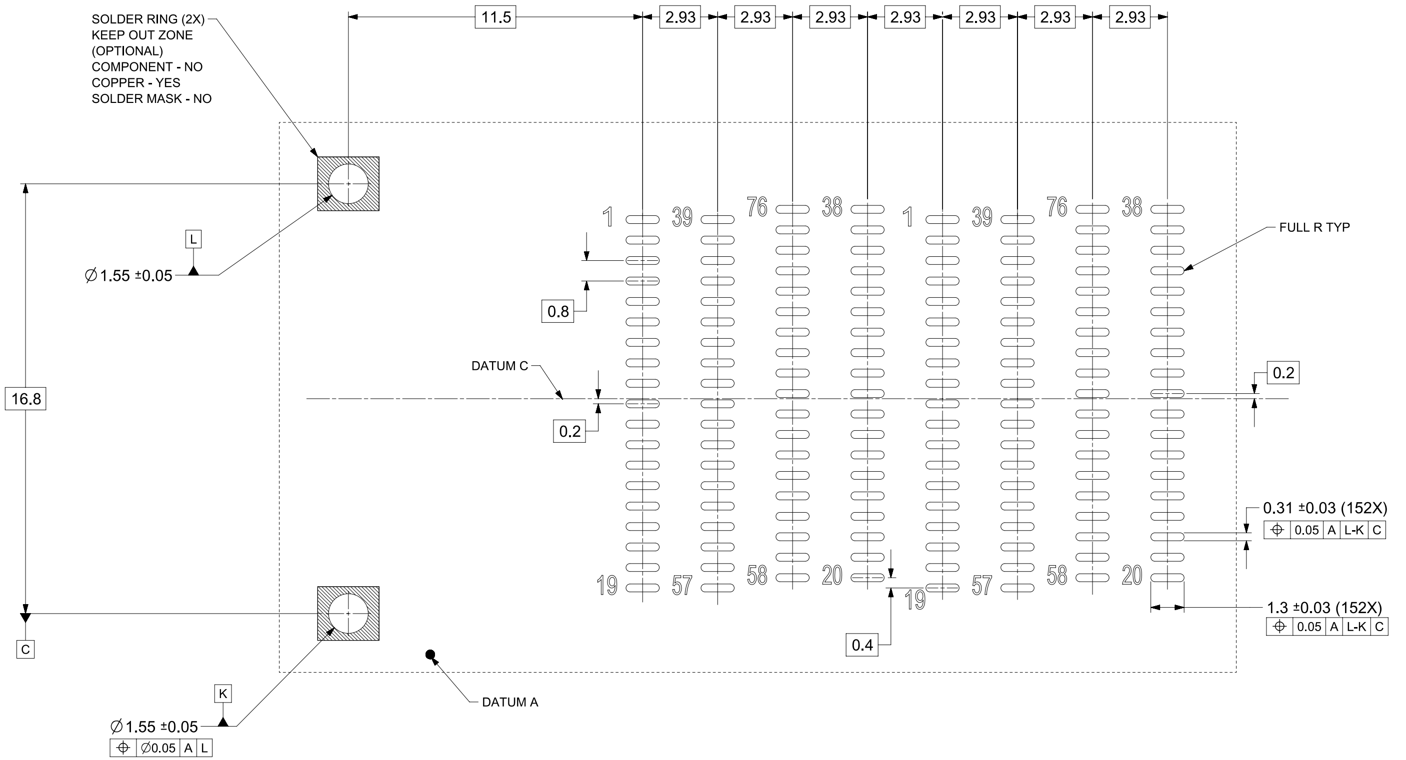


Figure 75: 2x1 SMT Connector and Cage PCB Layout with Solder Ring

1

2 **Figure 76: 2x1 SMT Connector and Cage PCB Layout with Press Fit**

3



1
2 **Figure 77: Detail QSFP1600 2x1 SMT connector host layout**
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8 QSFP-DD1600 Mechanical and Board Definition

Some of the QSFP-DD1600 module mechanical specifications are common with QSFP-DD/QSFP-DD800, below are the list of relevant QSFP-DD/QSFP-DD800 sections applicable to QSFP-DD1600:

- 6.1 Introduction to QSFP-DD/QSFP-DD800/QSFP-DD1600 Modules
- 6.2 Datums, Dimensions and Component Alignment
- 6.3 Module Form Factors for QSFP-DD/QSFP-DD800/QSFP-DD1600
- 6.4 Module Flatness and Roughness
- 6.6 Module Extraction and Retention Forces
- 6.8 QSFP-DD Surface Mount Electrical Connector Mechanical
- 7.2 QSFP-DD800 module mechanical dimensions.

8.1 Introduction

The module paddle card dimensions of the QSFP-DD1600 have been improved to support 224 Gb/s PAM4 (112 GBd) serial data rate.

QSFP-DD1600 supports multiple connector/cage form factors. QSFP-DD1600 cages and connectors are compatible with QSFP-DD/QSFP-DD800 cages/connectors/modules, QSFP-DD1600 cages/connectors also accepts QSFP+ family of modules. Example of QSFP-DD1600 connector/cage system are:

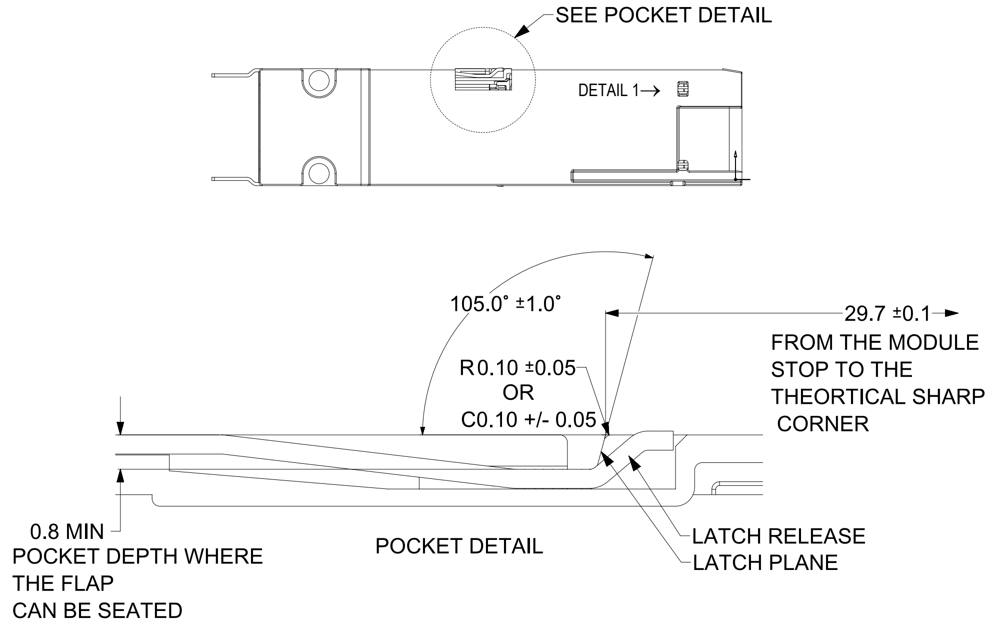
- 1x1 surface mount connector/cage
- 2x1 surface mount connector/cage.

8.2 QSFP-DD1600 module mechanical dimensions

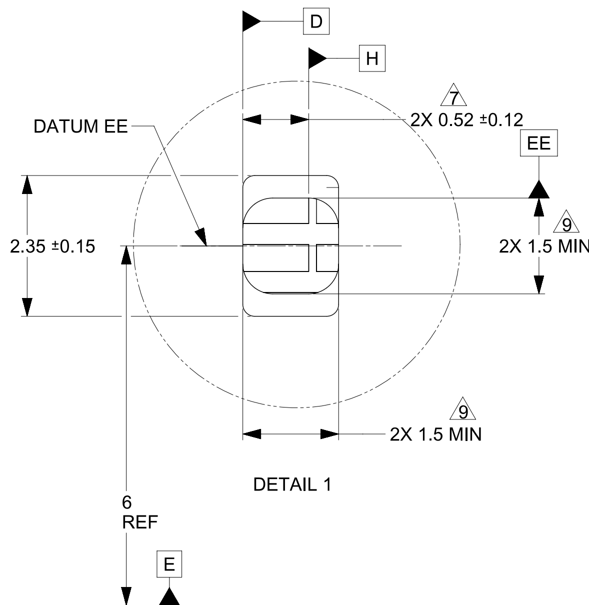
QSFP-DD1600 module mechanical dimensions are based on QSFP-DD800 mechanical in section 7.2, with based drawing shown in Figure 63 and Figure 64. QSFP-DD1600 improved module latch pocket is shown in Figure 78 and the module leading edge Detail 1 shown in Figure 79.

Appendix F shows a thermally improved QSFP-DD1600 module design with bottom heat sink and PCB cut-out.

1



2
3 **Figure 78: QSFP-DD1600 module latch pocket**
4



5
6 **Figure 79: QSFP-DD1600 Detail 1**
7
8

1
8.3 QSFP-DD1600 improved module paddle card dimensions

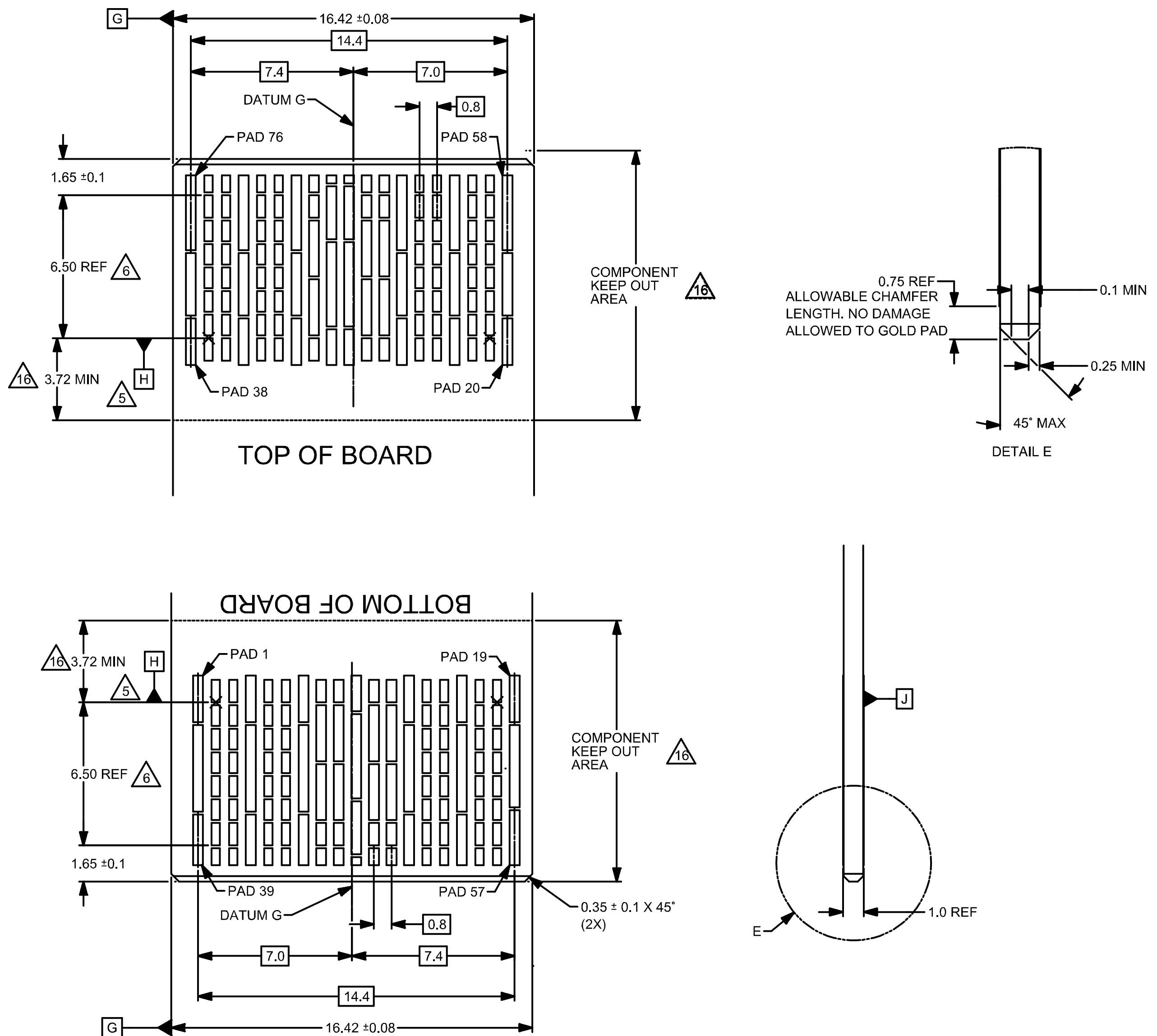
2 The QSFP-DD1600 module paddle card pre-wipe and signal pad have a tighter tolerance to support 224 Gb/s
3 PAM4 (112 GBd) serial data rates, all other dimension are identical to QSFP-DD800 paddle card Figure 66
4 and Figure 67. QSFP-DD1600 module improved paddle card dimensions shown in Figure 80 and the detail
5 module paddle card dimension shown in Figure 81.

NOTES APPLY TO MODULE PADDLE CARD:

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD
5. DATUM H IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTERMOST SIGNAL CONTACT PADS TO BE RE-ESTABLISHED ON EACH SIDE.
6. DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS
7. DIMENSION AND TOLERANCE APPLIES TO ALL GROUND PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
8. DIMENSION AND TOLERANCE APPLIES TO ALL POWER PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
9. DIMENSION AND TOLERANCE APPLIES TO ALL HIGH SPEED SIGNAL PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD
10. A ZERO GAP IS ALLOWED FOR A CONTINUOUS SIGNAL PADS ON BOTH TOP AND BOTTOM
11. APPLIES TO ALL SIGNAL PAD TO PRE-WIPE SPACING.
12. PRE-WIPE PADS (SHADED AREA), ON MODULE CARD HOST ARE OPTIONAL
13. PRE-WIPE PADS (UNSHADED AREA), ARE REQUIRED EXCEPT IN CONTINUOUS POWER AND GROUND DESIGNS
14. PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS MUST NOT BE PROUD OF THE PAD SURFACE
15. MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS
16. COMPONENT KEEP OUT AREA MUST MEASURE FROM DATUM H
17. A FIVE PRE-WIPE PAD CONFIGURATION IS REQUIRED AND THE PADS SHALL BE SEPARATED WITH A GAP OF 0.13+/-0.05
18. CONTACT PAD PLATING
    0.38 MICROMETERS MINIMUM GOLD OVER
    1.27 MICROMETERS MINIMUM NICKEL
    ALTERNATE CONTACT PAD PLATING
    0.05 MICROMETERS MINIMUM GOLD OVER
    0.30 MICROMETERS MINIMUM PALLADIUM OVER
    1.27 MICROMETERS MINIMUM NICKEL
19. DIMENSION AND TOLERANCE APPLIES TO ALL LOW SPEED SIGNAL PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD

6

1



2
3 **Figure 80: QSFP-DD1600 improved module paddle card dimension**

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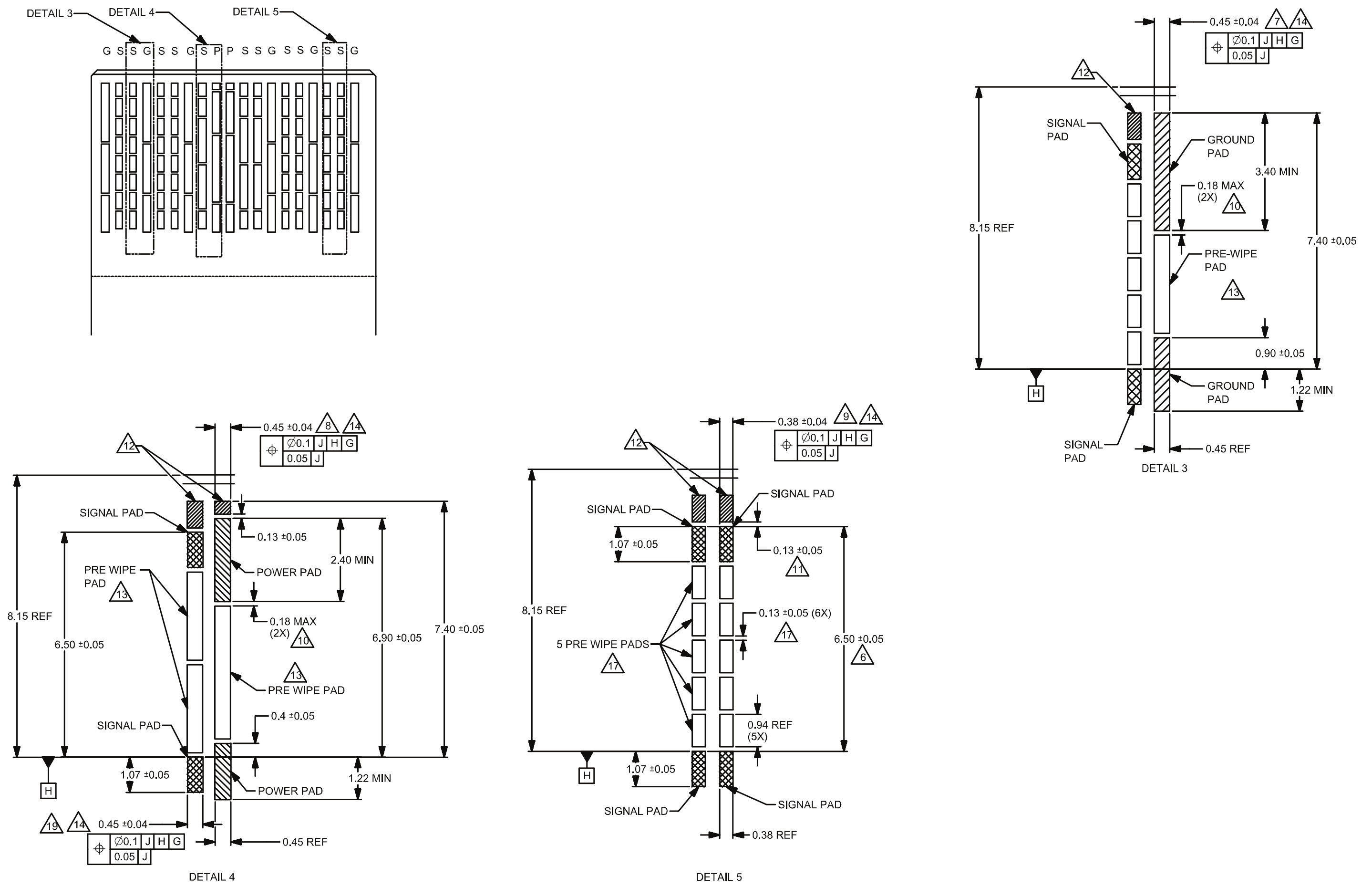


5
6 **Figure 81: QSFP-DD1600 improved detail module paddle card dimensions**
7

1 ## 8.4 QSFP-DD1600 1x1 SMT connector/cage system

2 The 1x1 SMT connector/cage mechanical outline for QSFP-DD1600 is similar to the QSFP-DD 1x1
3 connector/cage, see 6.8, but single contact ground host pads are replaced with dual ground host pads to
4 decrease the crosstalk.

5 ### 8.4.1 Surface mount connector and cage host PCB layout

6 A typical host board mechanical layout for attaching the QSFP-DD1600 surface mount Connector and Cage
7 System is shown in Figure 68. Location of the pattern on the host board is application specific.
8
9 To achieve 224 Gbps (112 GBd) operation the QSFP-DD1600 pad dimensions and associated tolerances
10 have been improved as compared to QSFP-DD800, and one must adhere and pay attention to the host board
11 layout.
12
13 Notes for host PCB requirements (see Figure 68):

1. THE ENTIRE AREA UNDER THE CONDUCTOR (INSIDE DASHED LINES), IS TO BE CONSIDERED A KEEP OUT AREA FOR COMPONENTS.

2 HATCHED AREAS SHOULD REPRESENT ZONES ON THE PCB THAT COME IN CONTACT WITH OR CLOSE PROXIMITY TO THE PLASTIC HOUSING OR THE CONNECTOR CAGE. INDICATED AREAS TO BE CONSIDERED TRACE FREE.

14

15
16
17 **Figure 82: QSFP-DD1600 reduced pad SMT host PCB layout**
18

8.4.2 QSFP-DD1600 Host Pad Assignment

For improved crosstalk QSFP-DD1600 host connector pads have dual grounds, see Figure 83. QSFP-DD1600 connector/cage systems are backward compatible with QSFP-DD/QSFP-DD800/QSFP+ family of modules. Within the QSFP-DD1600 connector/cage system ground pads at the paddle card transition into dual host ground pads. QSFP-DD1600 paddle card pad assignment is identical to QSFP-DD family of form factors, see Figure 2. Within the QSFP-DD1600 connector/cage system ground pads at the paddle card transition into dual host ground pads, in addition VccRx, VccRx1, VccTx1, and VccTx also transition to being dual host pads.

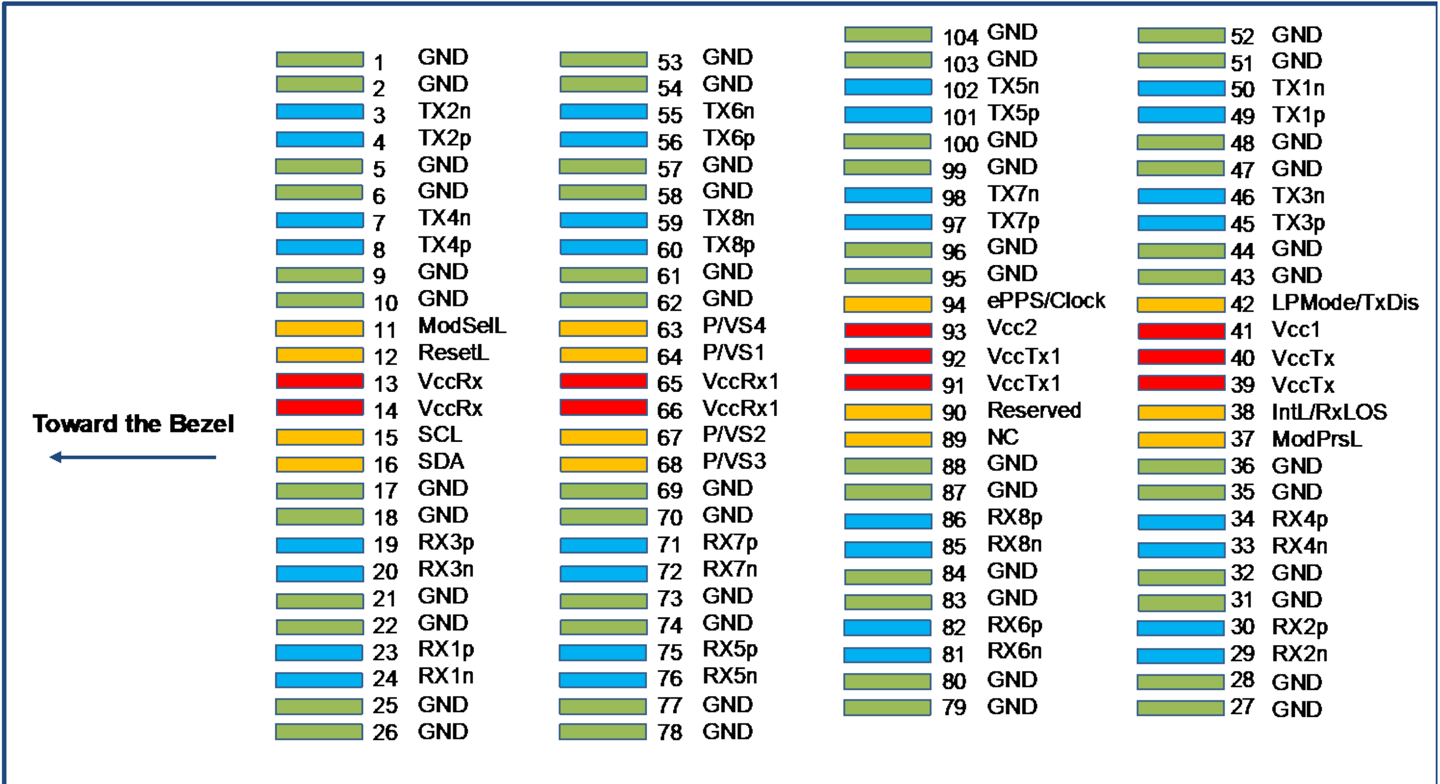


Figure 83: QSFP-DD1600 Host Pad Assignment

8.4.3 QSFP-DD1600 Surface Mount Electrical Connector Mechanical

The QSFP-DD1600 Connector is a 76-contact, right angle edge connector compatible with QSFP-DD interface specifications in Figure 71. The SMT connector in a 1xN cage is shown in Figure 55 with detailed drawings shown in Figure 56, Figure 57, and Figure 59 (FRONT VIEW only). For recommendations of the SMT cage bezel opening, see Figure 60. QSFP-DD1600 SMT connector view and connector detail designs are shown in Figure 84.

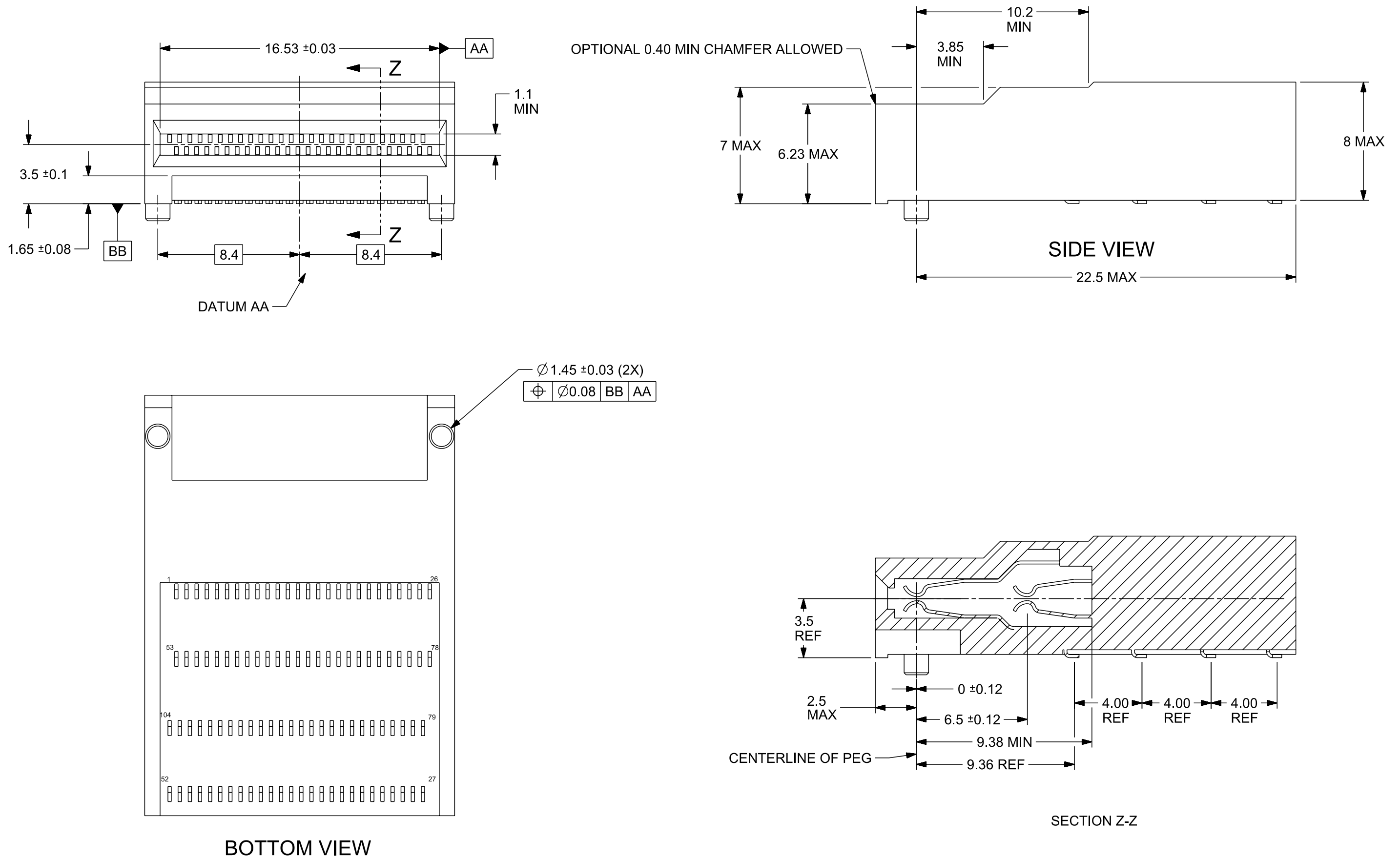
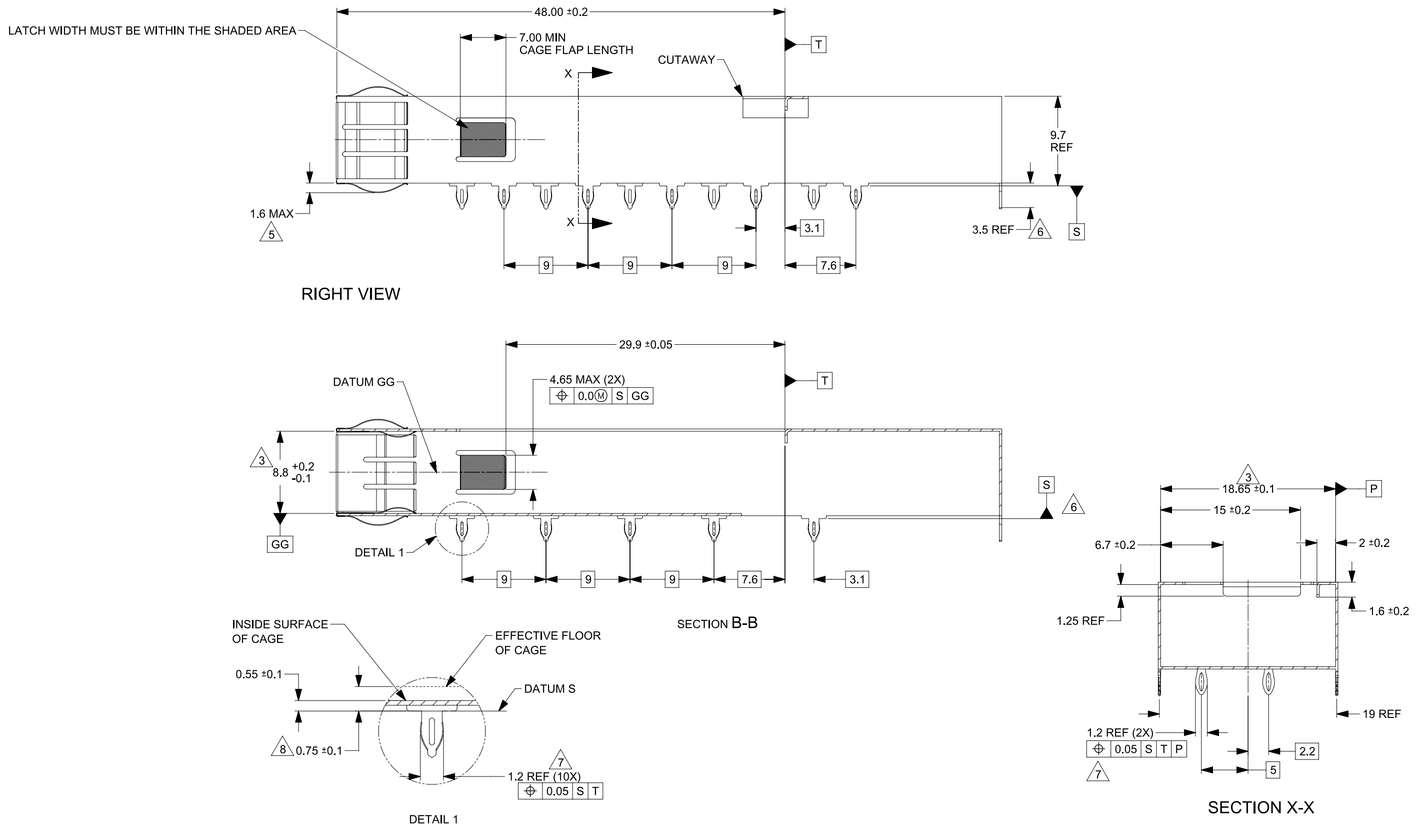


Figure 84: QSFP-DD1600 SMT 1x1 connector detail design

1 ### 8.4.4 QSFP-DD1600 Cage Flap

2 For QSFP-DD1600 SMT 1xN cage drawing detail drawings, see Figure 56 and Figure 58. For improved
3 QSFP-DD1600 cage flap see Figure 85.



4
5 **Figure 85: QSFP-DD1600 Cage Flap**
6

8.5 2x1 Surface Mount Technology (SMT) Connector/Cage

The QSFP-DD1600 2x1 SMT connector/cage mechanical outline has similar dimensions as the QSFP-DD 2x1 press fit connector/cage, see 6.7.

8.5.1 2x1 SMT Connector/Cage System

Each of the QSFP-DD1600 stacked connectors are 76-contacts right angle connectors on 0.8mm pitch with double grounds inside the connector that fan out to 104 pcb contacts on 0.6mm pitch. In addition, for QSFP-DD 1600, the upper and lower ports have been separated by 1.87mm to allow for better thermal management of the lower port, see Appendix F for further details. A typical host board mechanical layout for attaching the QSFP-DD1600 surface mount connector and cage system are shown in Figure 86 and Figure 87. The QSFP-DD1600 connector and cage supports single host PCB implementations, see Figure 92 and Figure 93.

To achieve 224 Gbps (112 GBd) operation the QSFP-DD1600 pad dimensions and associated tolerances have improved compared to QSFP-DD800 and one must adhere and pay attention to the host board layout.

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

△3 DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED

△4 CONNECTOR REMOVED FOR CLARITY

△5 APPLIES TO ALL SPRING FINGERS ON ALL SIDES

△6 EXTERNAL CAGE DIMENSIONS DOES, NOT INCLUDE FOLDING TABS

△7 LENGTH OF CAGE AND SIGNAL TAILS

△8 PRESS FIT CAGE PINS APPLY TO RIGHT SIDE OF CAGE

△9 PRESS FIT CAGE PINS APPLY TO LEFT SIDE OF CAGE

△10 PRESS FIT OFFSET BETWEEN RIGHT AND LEFT SIDE OF CAGE

△11 DIMENSIONS INCLUDE BACKCOVER

△12 SIZE AND POSITION OF CAGE AND CONNECTOR PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FORMAT FOOTPRINT LAYOUT

△13 CAVITY FOR HEATSINK IS OPTIONAL

△14 CONTACT PIN DIMENSION MEASURED FROM DATUM T.

△15 CONTACT PIN DIMENSION MEASURED FROM DATUM T1.

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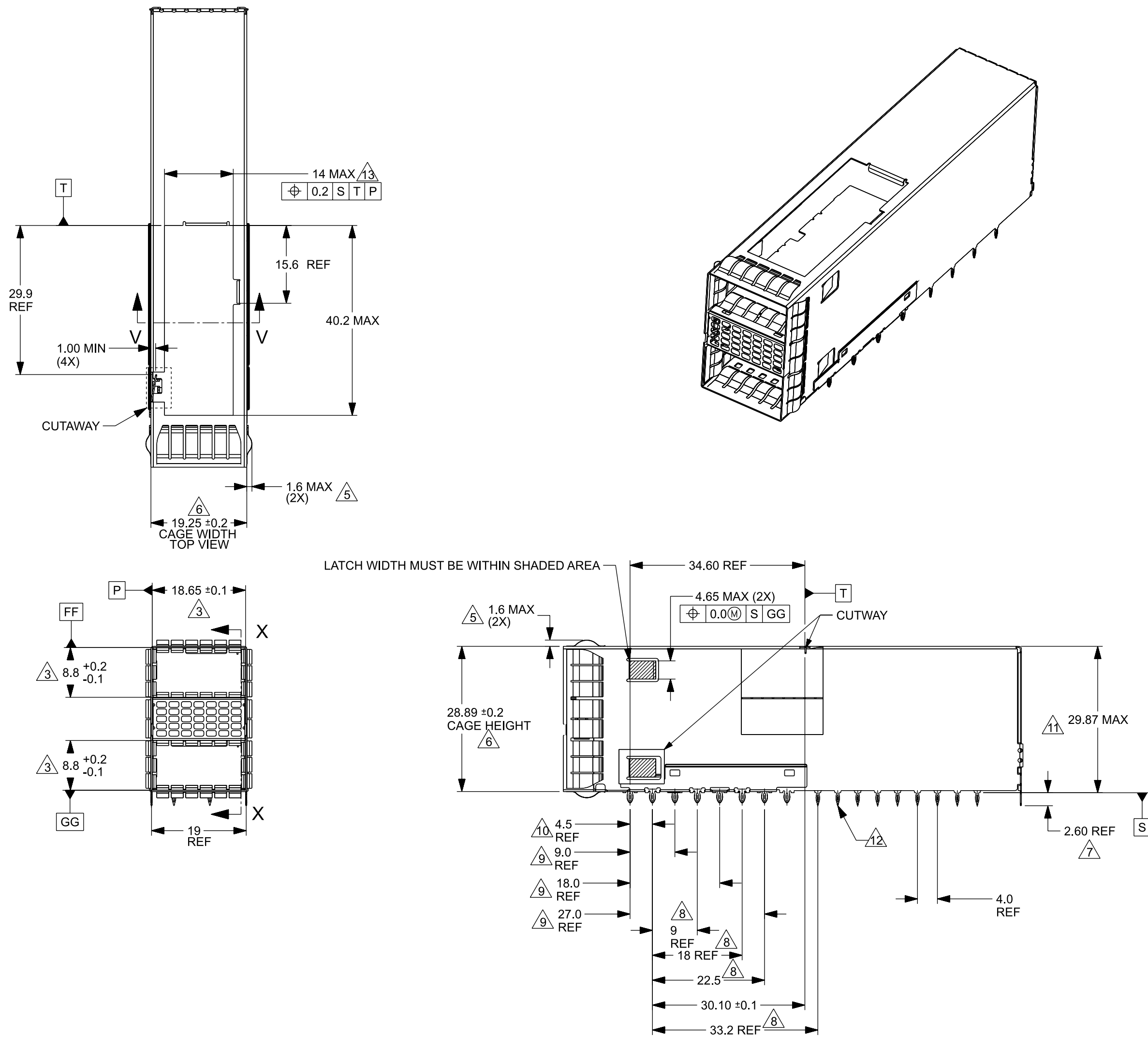

Figure 86: QSFP-DD1600 2x1 SMT Stack Cage

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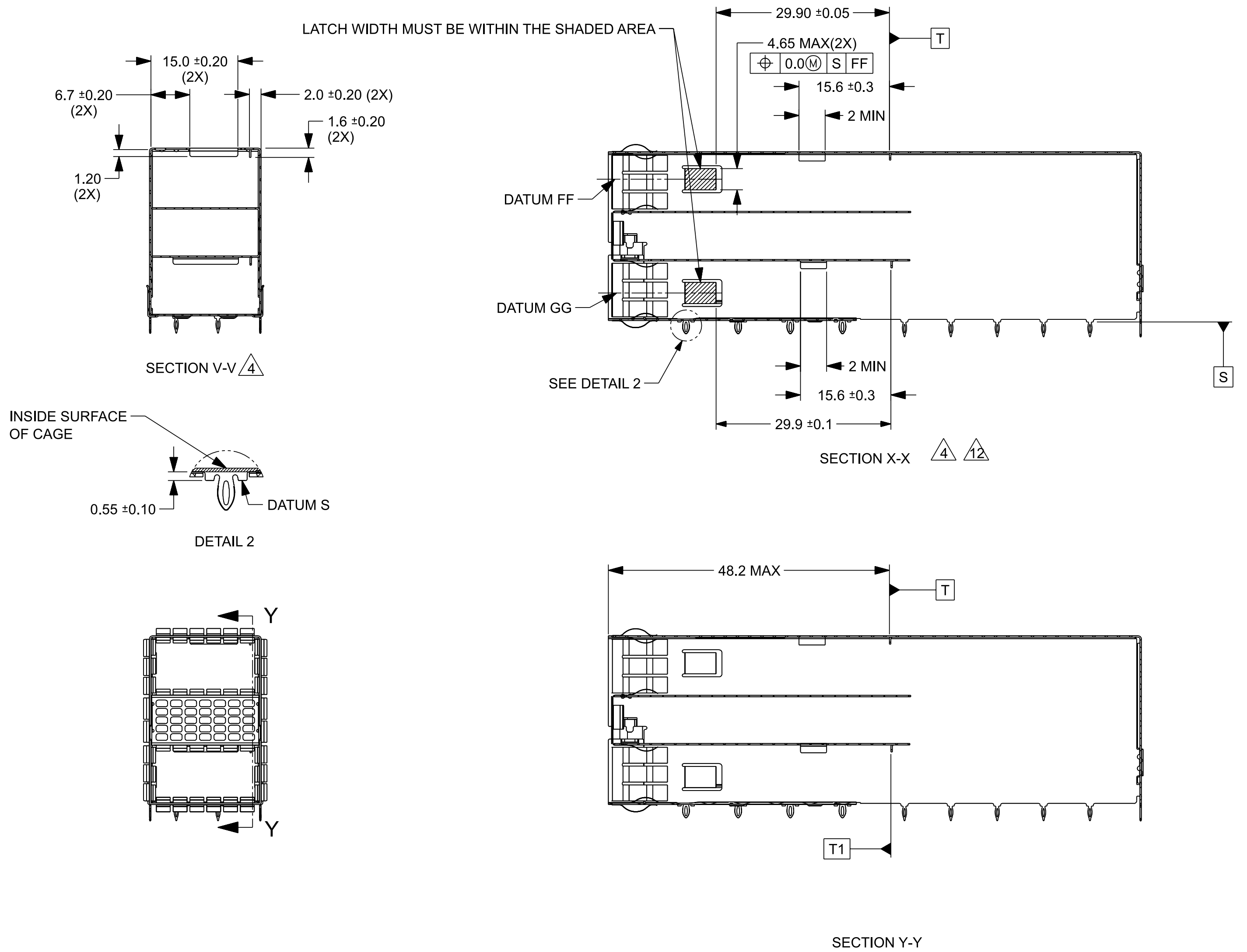

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Figure 87: QSFP-DD1600 2x1 SMT cage dimensions
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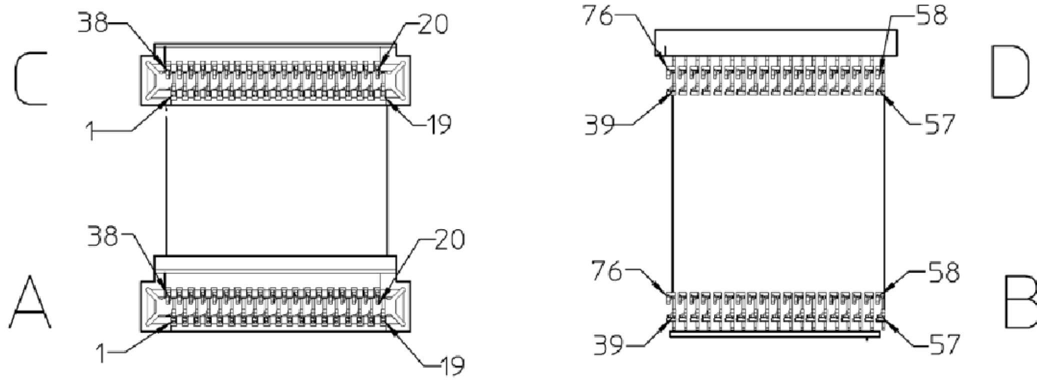
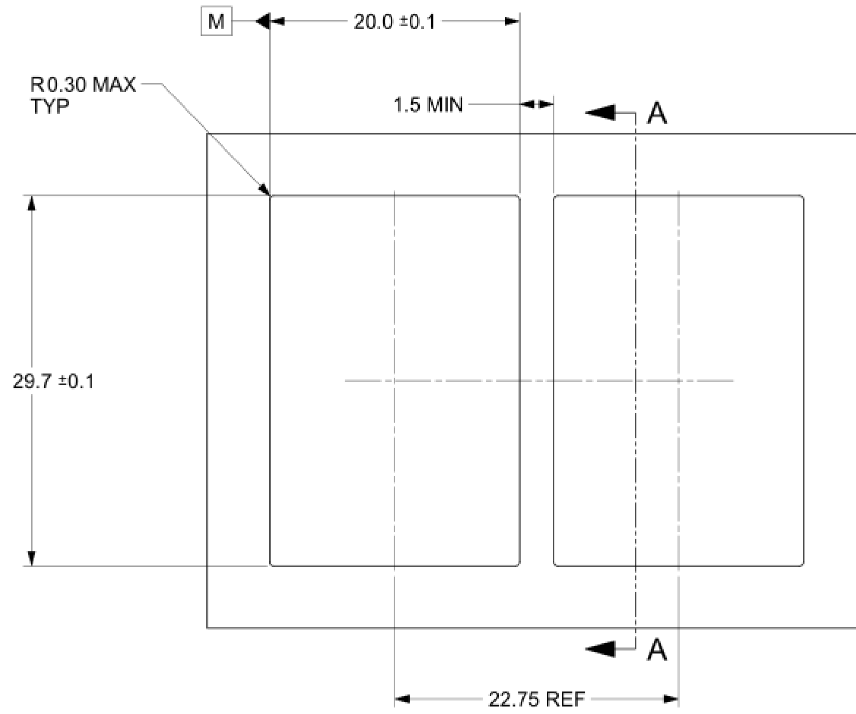
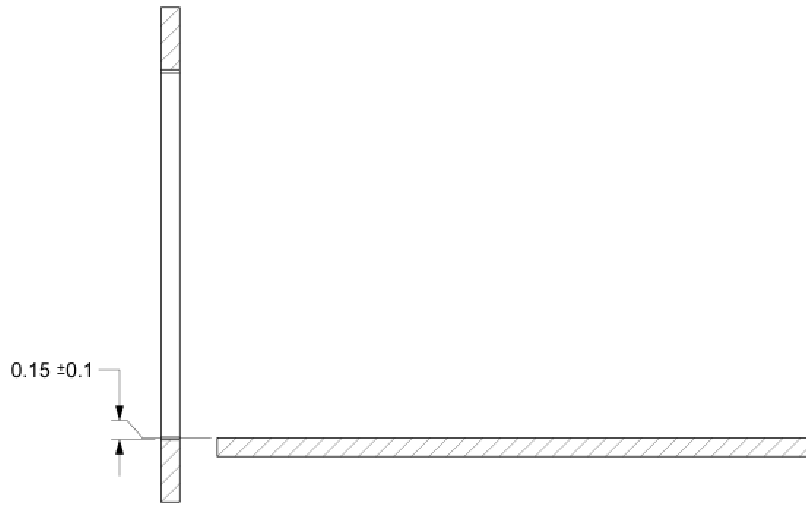


2
3 **Figure 88: Connector pads in 2x1 SMT stacked cage as viewed from front**
4





SECTION A-A

1
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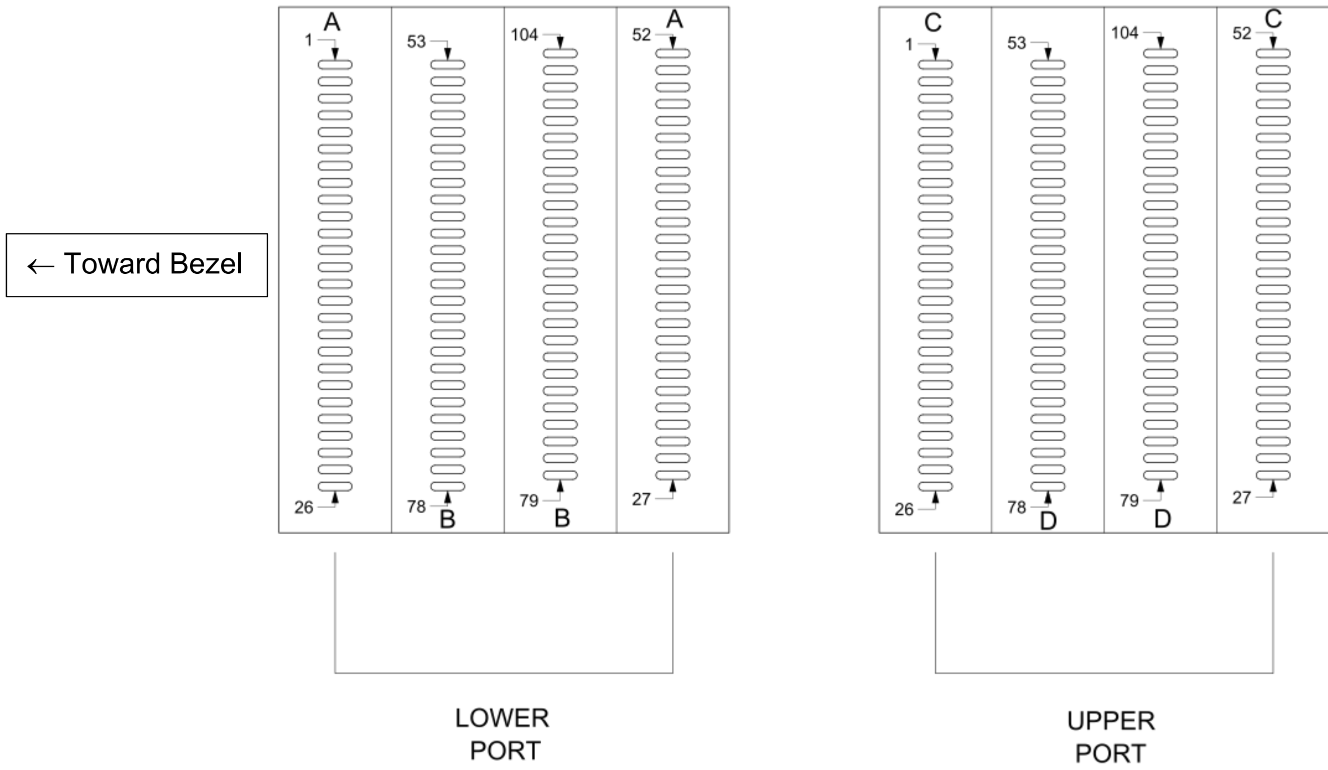
Figure 89: QSFP-DD1600 2x1 SMT Bezel Opening



1
2 **Figure 90: 2x1 SMT Pads Labeling**
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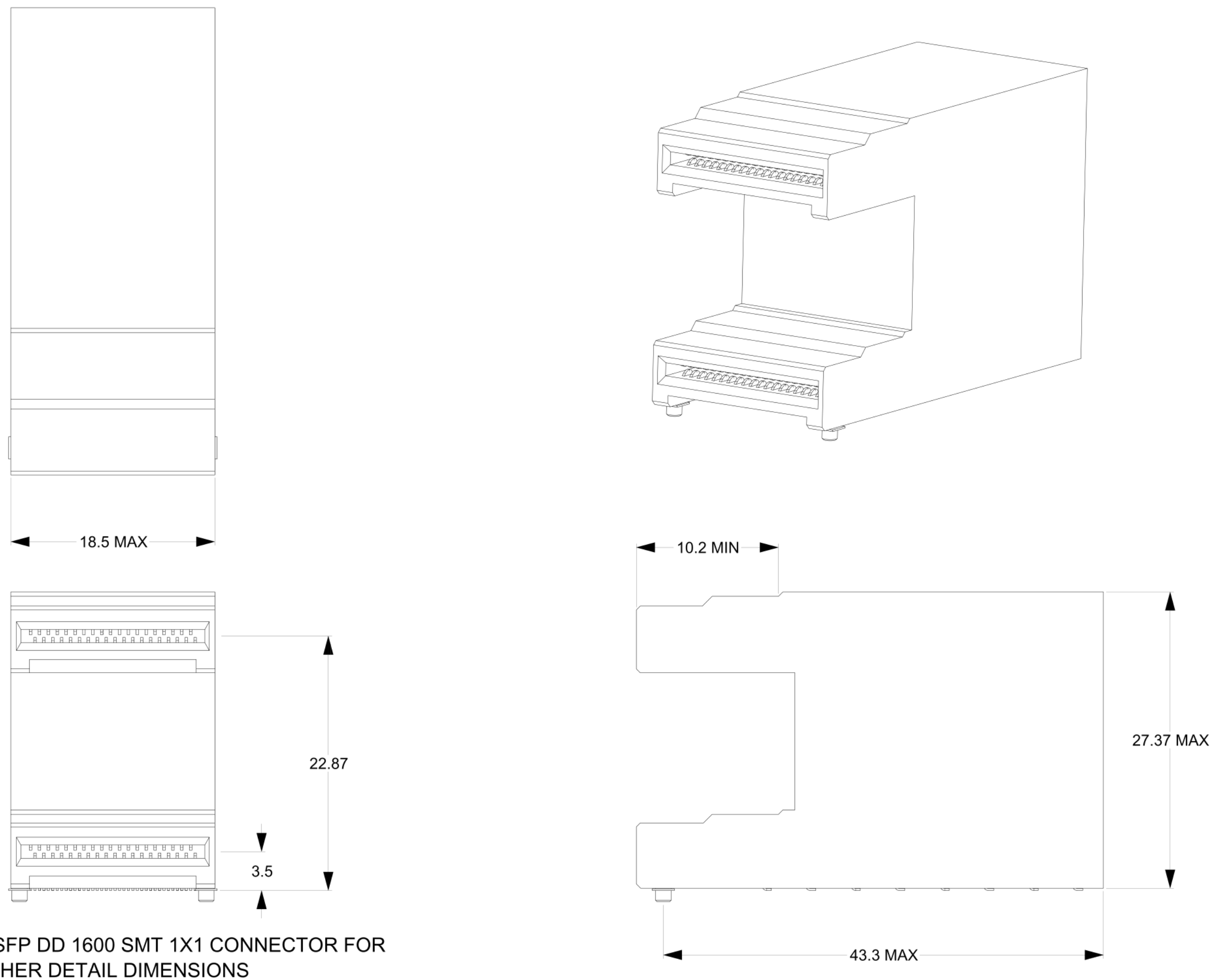
1 **8.5.2 2x1 SMT Connector and Cage host PCB layout**

2 The QSFP-DD1600 2x1 stack connector system shown in Figure 91, for all other dimensions see QSFP-
3 DD1600 1x1 SMT connector Figure 84. Connector and cage system shown in Figure 92. The detail host PCB
4 layout for QSFP-DD1600 is shown in Figure 93Figure 77. Location of the pattern on the host board is
5 application specific. To achieve 224 Gbps (112 GBd) operation pad dimensions and associated tolerance
6 must be adhered to and attention paid to the host layout.

7



8

9 **Figure 91: QSFP-DD1600 stacked SMT 2x1 connector**

10

11

Notes for host PCB requirements (see Figure 75, Figure 76, and Figure 77):

1. THE ENTIRE AREA UNDER THE CONDUCTOR (INSIDE DASHED LINES), IS TO BE CONSIDERED A KEEP OUT AREA FOR COMPONENTS.

2. HATCHED AREAS SHOULD REPRESENT ZONES ON THE PCB THAT COME IN CONTACT WITH OR CLOSE PROXIMITY TO THE PLASTIC HOUSING OR THE CONNECTOR CAGE. INDICATED AREAS TO BE CONSIDERED TRACE FREE.

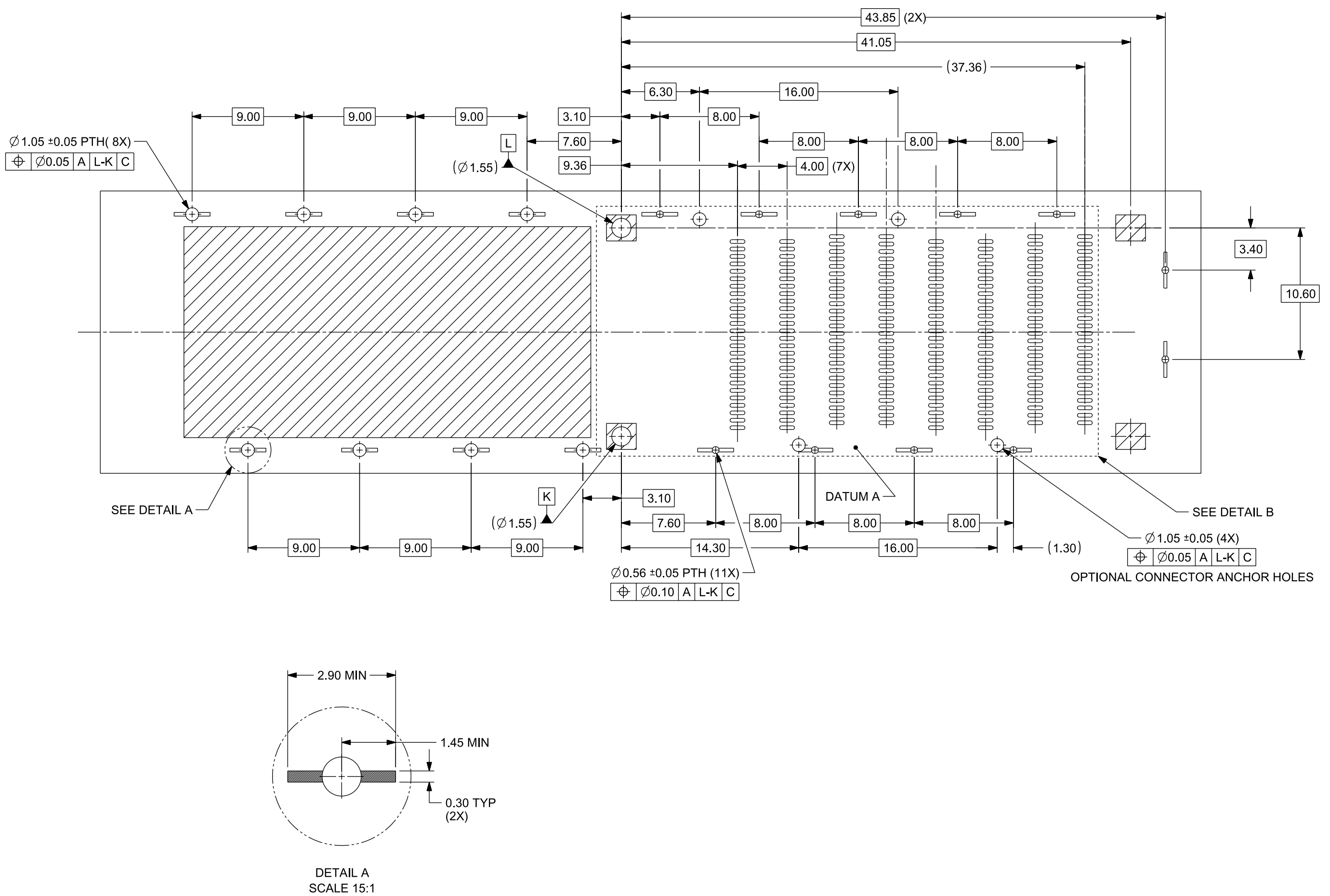
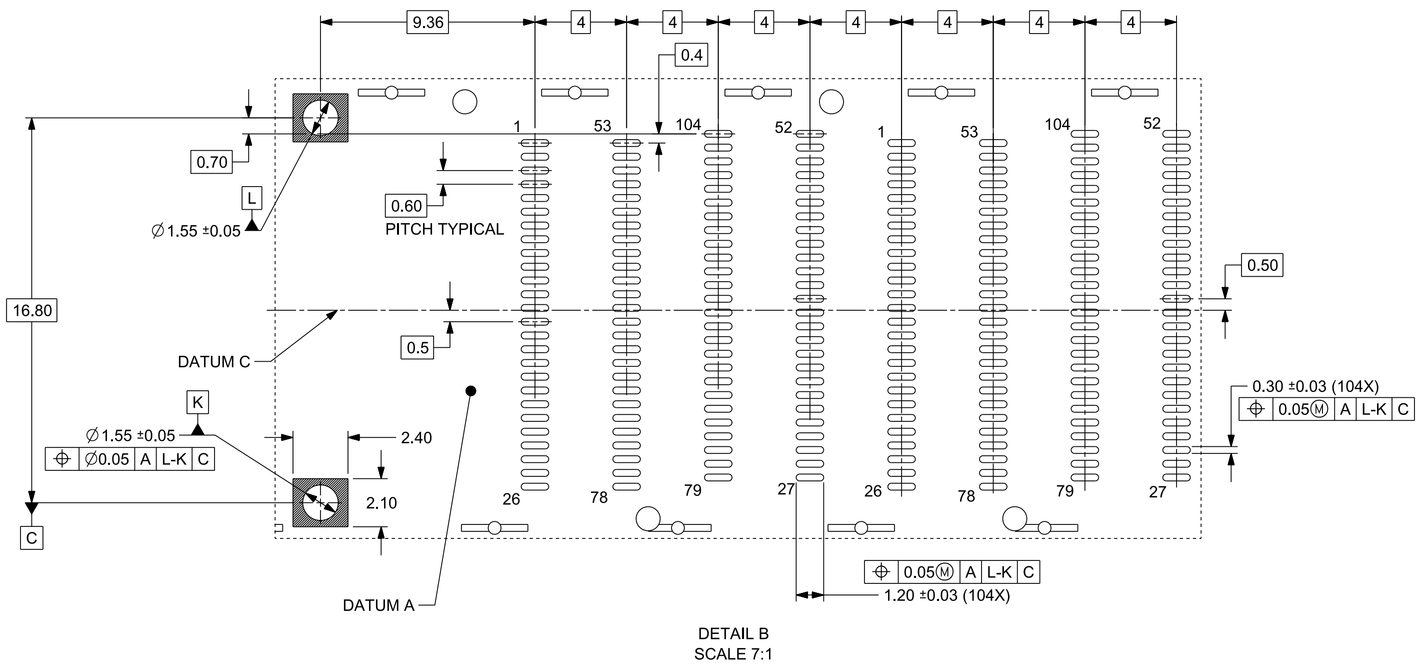


Figure 92: 2x1 SMT Connector and Cage PCB Layout



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3 **Figure 93: Detail QSFP1600 2x1 SMT connector host layout**
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9 Module Environmental and Thermal Requirements

The QSFP-DD/QSFP-DD800/QSFP-DD1600 modules are designed to allow for up to 36 modules; stacked, ganged and/or belly-to-belly in a 1U 19" rack, with the appropriate thermal design for cooling/airflow.

The equipment supplier is responsible for controlling the module case temperature to the specified range. The module supplier is responsible for defining a point on the module case where the temperature is measured. This should be a point connected to an internal component with the least thermal margin, e.g., a laser diode. It is recommended that the defined point on the module case be behind the equipment faceplate to enable in-system monitoring.

9.1 Thermal Requirements

The module case temperature may be within one or more of the case temperatures ranges defined in Table 19. The temperature ranges are applicable between 60 m below sea level and 1800 m above sea level, utilizing the host systems designed airflow. For further information see Telcordia GR-63-CORE, Issue 5, December 2017, NEBSTM Requirements: Physical Protection.

Table 19- Temperature Range Class of operation

Class	Module Case Temperature
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

9.2 Thermal Requirements – tighter controlled environments

The classes in Table 20 are intended for tighter controlled environments, e.g., data center environments as described in *“Thermal guidelines for data processing environments”, fourth Ed., ASHRAE, 2015.* The four classes correspond to different ranges of equipment intake air temperature.

Table 20- Temperature Range Classes for Tighter Controlled Applications

Class	Module Functional Case Temperature[1]	Module Case Temperature[2]
A1	15°C to 62°C	25°C to 62°C
A2	10°C to 65°C	20°C to 65°C
A3	5°C to 70°C	15°C to 70°C
A4	5°C to 75°C	15°C to 75°C

Notes:
1. Functional includes all features available in Low Power Mode.
2. Module case temperature means all specifications are met in high power mode.

9.3 External Case and Handle Touch Temperature

For all power classes, all module case and handle surfaces outside of the cage must comply with applicable touch temperature requirements. If the module case temperature will exceed applicable short-term touch temperature limits, a means must be provided to prevent contact with the case during unlatching and removal. Figure 33 and Appendix B show typical handles used to unlatch and remove the module, thereby limiting contact with the module case. Handles are typically low thermal conductivity elastomer and allow for a higher touch temperature, see IEC/UL 60950-1 [8] and Telcordia GR-63-CORE [23].

9.4 Supplemental Thermal Characteristics for high power modules (optional)

In high power modules, the module implementer needs to ensure that the module meets all performance and reliability specifications and monitoring only the case temperature can result in overly conservative readings for the host equipment to use. Instead by monitoring all necessary internal component temperature sensors against their high temperature warning/alarm/shutdown limits, the module and host equipment can more accurately assess the component's margin to the various temperature limits that affect performance and reliability. To be compatible with the existing CMIS approach to report the case temperature Tcase, it is possible to convert these multiple sensor readings in such a way to provide the host equipment the ability to manage the system and module cooling without a change to CMIS software. The specific temperature sensors, including their values, thresholds and physical location are defined and known by the module implementor, and are not required to be advertised to the equipment supplier. Instead, the module's firmware shall process the monitored temperature data points against their limits, and provide the following to the equipment supplier via the management interface:

I. A high temperature monitor, which shall be a single monotonic increasing/decreasing value and be a consolidated leading indicator for all the module's defined sensor points against their high temperature thresholds (including warning, alarm, shutdown).

II. Module implementor's defined limits for the high temperature monitor values, including warning, alarm and shutdown thresholds are known. The least margin to these limits shall be advertised to the equipment supplier as the equivalent margin to the advertised case temperature limit via the management interface. The module's specified case temperature limits are recommended (but not required) to be consistent with temperature ranges classes defined in Section 9.1.

The temperature monitors are expected to represent an accurate measurement of where the module operates relative to the temperature limits defined by the module supplier. The temperature monitors are not expected to represent a physical temperature at any specified location on or inside the module.

9.4.1 Example procedure to implement high power module monitoring

As an example, a procedure to calculate the high temperature case monitor temperature alarm threshold that is reported by the module in CMIS to the host is outlined below in a case where 3 temperature sensors are being monitored by the module firmware (laser, DSP, TIA):

- Step I:
  The module's case temperature monitored sensor reading (Tcase) should have internal module specified thresholds that are advertised via the management interface:
  $Tcase_{warning\ threshold}$ *:Module case temperature warning threshold (for example 70 ºC)*
  $Tcase_{alarm\ threshold}$ *: Module case temperature alarm threshold (for example 75 ºC)*
  $Tcase_{shutdown\ threshold}$ *: Module case temperature shutdown threshold (for example 80 ºC)*

- Step II:
  Including all monitored sensors, calculate the temperature margin for the leading indicator against the module's known internal warning, alarm and shutdown thresholds.
  $margin_{warning} = \min(\Delta t_{laser,\ warning}, \Delta t_{DSP,warning}, \Delta t_{tia,warning}, \ldots \text{ etc.})$
  $margin_{alarm} = \min(\Delta t_{laser,\ alarm}, \Delta t_{DSP,alarm}, \Delta t_{tia,alarm}, \ldots \text{ etc.})$
  $margin_{shutdown} = \min(\Delta t_{laser,\ shutdown}, \Delta t_{DSP,shutdown}, \Delta t_{tia,shutdown}, \ldots \text{ etc.})$
  Where $\Delta t_{A,B}$ is the temperature margin for sensor A against its high temperature B threshold (where B can be the warning, alarm or shutdown temperature threshold).

  The calculation of the reported case temperature reading (Tcase) should be agnostic to how the module design defines the temperature thresholds of the monitored sensors, including temperature steps between warning, alarm and shutdown thresholds. One implementation that can accomplish this is outlined in step III below.

- Step III:
  Based on the margin with the smallest value greater or equal to zero, calculate the reported Tcase as below.
  If $margin_{warning}$ is the smallest margin, greater or equal to 0:
  $Tcase_{warning} = Tcase_{warning\ threshold} - margin_{warning}$
  If $margin_{alarm}$ is the smallest margin, greater or equal to 0:

$$Tcase_{\text{warning}} = Tcase_{\text{alarm threshold}} - margin_{\text{alarm}} * \frac{Tcase_{\text{alarm}} - Tcase_{\text{warning}}}{t_{\text{A,alarm}} - t_{\text{A,warning}}}$$

  where $t_{\text{A,alarm}}$ and $t_{\text{A,warning}}$ are the alarm and warning thresholds for the leading alarm threshold indicator, A, respectively with the smallest margin.
  If $margin_{shutdown}$ is the smallest margin, greater or equal to 0:

$$Tcase_{\text{warning}} = Tcase_{\text{shutdown threshold}} - margin_{\text{shutdown}} * \frac{Tcase_{\text{shutdown}} - Tcase_{\text{alarm}}}{t_{\text{A,shutdown}} - t_{\text{A,alarm}}}$$

  where $t_{\text{A,shutdown}}$ and $t_{\text{A,alarm}}$ are the alarm and warning thresholds for the leading alarm threshold indicator, A, respectively with the smallest margin.

Appendix A Normative Module and Connector Performance Requirements

A.1 QSFP-DD/QSFP-DD800/QSFP-DD1600 Performance Tables

EIA-364-1000 [6] shall be used to define the test sequences and procedures for evaluating the QSFP-DD/QSFP-DD800/QSFP-DD1600 connector systems described in this document. Where multiple test options are available, the manufacturer shall select the appropriate option where not previously specified. The selected procedure should be noted when reporting data. If there are conflicting requirements or test procedures between EIA-364 procedures and those contained within this document, this document shall be considered the prevailing authority. Unless otherwise specified, procedures for sample size, data, and collection to be followed as specified in EIA-364-1000. See EIA-364-1000 Annex B for objectives of tests and test groups.

This document represents the minimum requirements for the defined product. Additional test conditions and evaluations may be conducted within the defined EIA-364-1000 sequences. More extreme test conditions and failure criteria may be imposed and still meet the requirements of this document.

A.2 Test

Table 21 summarizes the performance criteria that are to be satisfied by the connector described in this document. Most performance criteria are validated by EIA-364-1000 testing, but this test suite leaves some test details to be determined. To ensure that testing is repeatable, these details are identified in Table 22. Finally, testing procedures used to validate any performance criteria not included in EIA-364-1000 are provided in Table 23.

1
2 **Table 21- Form Factor Performance Requirements**

Performance Parameters	Description/ Details	Requirements
Mechanical/ Physical Tests		
Plating Type	Plating type on connector contacts	Precious (refer to 6.5 for plating details)
Surface Treatment	Surface treatment on connector contacts; if surface treatment is applied, Test Group 6 is required	Manufacturer to specify
Wipe length	Designed distance a contact traverses over a mating contact surface during mating and resting at a final position. If less than 0.127 mm, test group 6 is required	Manufacturer to specify
Rated Durability Cycles	The expected number of durability cycles a component is expected to encounter over the course of its life	Connector/ cage: 100 cycles Module: 50 cycles
Mating Force[1]	Amount of force needed to mate a module with a connector when latches are deactivated	QSFP module: 60 N MAX QSFP-DD module: 90 N MAX
Unmating Force[1]	Amount of forced needed to separate a module from a connector when latches are deactivated	QSFP module: 30 N MAX QSFP-DD module: 50 N MAX
Latch Retention[1]	Amount of force the latching mechanism can withstand without unmating	QSFP module: 90 N MIN QSFP-DD module: 90 N MIN
Cage Latch Strength[1]	The amount of force that the cage latches can hold without being damaged.	125 N MIN
Cage Retention to Host Board[1]	Amount of force a cage can withstand without separating from the host board	114 N MIN
Environmental Requirements		
Field Life	The expected service life for a component	10 years
Field Temperature[2]	The expected service temperature for a component	65°C
Electrical Requirements		
Current (see 4.7.1)	Maximum current to which a contact is exposed in use	0.5 A per signal contact MAX 1.5 A per power contact MAX 2.0 A (Single port QSFP-DD1600) per contact MAX
Operating Rating Voltage	Maximum voltage to which a contact is exposed in use	30 V DC per contact MAX
Note: 1. These performance criteria are not validated by EIA-364-1000 testing, see Table 23 for test procedures and pass/fail criteria. 2. Field temperature is the ambient air temperature around the component.		

3
4

1
2 Table 22 describes the details necessary to perform the tests described in the EIA-364-1000 test sequences.
3 Testing shall be done in accordance with EIA-364-1000 and the test procedures it identifies in such a way that
4 the parameters/ requirements defined in Table 21 are met. Any information in this table supersedes EIA-364-
5 1000.
6
7 **Table 22- EIA-364-1000 Test Details**

Performance Parameters	Description/ Details	Requirements
Mechanical/ Physical Tests		
Durability (preconditioning)	EIA-364-09 To be tested with connector, cage, and module. Latches may be locked out to aid in automated cycling.	No evidence of physical damage
Durability[1]	EIA-364-09 To be tested with connector, cage, and module. Latches may be locked out to aid in automated cycling.	No visual damage to mating interface or latching mechanism
Environmental Tests		
Cyclic Temperature and Humidity	EIA-364-31 Method IV omitting step 7a Test Duration B	No intermediate test criteria
Vibration	EIA-364-28 Test Condition V Test Condition Letter C Test set-up: Connectors may be restrained by a plate that replicates the system panel opening as defined in this specification. External cables may be constrained to a non-vibrating fixture a minimum of 8 inches from the module. For cabled connector solutions: Wires may be attached to PCB or fixed to a non-vibrating fixture.	No evidence of physical damage -AND- No discontinuities longer than 1 μs allowed
Mixed Flowing Gas	EIA-364-65 Class II See Table 4.1 in EIA-364-1000 for exposure times Test option Per EIA-364-1000 option 3	No intermediate test criteria
Electrical Tests		
Low Level Contact Resistance[2]	EIA-364-23 20 mV DC Max, 100 mA Max To include wire termination or connector-to-board termination	20 mΩ Max change from baseline
Dielectric Withstanding Voltage	EIA-364-20 Method B 300 VDC minimum for 1 minute Applied voltage may be product / application specific	No defect or breakdown between adjacent contacts -AND- 1 mA Max Leakage Current
Notes: 1. If the durability requirement on the connector is greater than that of the module, modules may be replaced after their specified durability rating. 2. The first low level contact resistance reading in each test sequence is used to determine a baseline measurement. Subsequent measurements in each sequence are measured against this baseline.		

8
9

Table 23 describes the testing procedures necessary to validate performance criteria not validated by EIA-364-1000 testing. The tests are to be performed in such a way that the parameters/ requirements defined in Table 21 are met.

Table 23- Additional Test Procedures

Tests	Test Descriptions and Details	Pass/ Fail Criteria
Mechanical/ Physical Tests		
Mating Force[1] Unmating Force[1]	EIA-364-13 To be tested with cage, connector, and module. Latching mechanism deactivated (locked out).	Refer to Table 21 -AND- No physical damage to any components
Latch Retention[1]	EIA-364-13 To be tested with cage, connector, and module. Latching mechanism engaged (not locked out).	
Latch Strength	An axial load applied using a static load or ramped loading to the specified load. To be tested with cage, connector, and module or module representative tool without heat sinks Latching mechanism engaged (not locked out).	
Cage Retention to Host Board	Tested with module, module analog, or fixtures mated to cage. Pull cage in a direction perpendicular to the board at a rate of 25.4mm/min to the specified force.	No physical damage to any components -AND- Cage shall not separate from board
Electrical Tests		
Current	EIA-364-70 Method 3, 30-degree temperature rise Contacts energized: All signal and power contacts energized simultaneously	Refer to Table 21 for current magnitude

Note:
1. Values listed in Table 21 apply with or without the presence of a riding heat sink.

Appendix B Informative overall module length with elastomeric handle

Figure 94 and Figure 95 show flexible elastomeric handles attached to the QSFP-DD/QSFP-DD800 module latches (13.5 mm REF is the height of latch and not the heartsink). Handle ends for Types 1, Type 2A, and, Type 2B modules should be aligned independent of module case extension. Type 1 modules should meet the overall length of 118 mm maximum per Figure 94 with a handle length of approximately 50mm. Type 2 modules should comply with Figure 95 and have reduced handle length equal to the module case length extension.

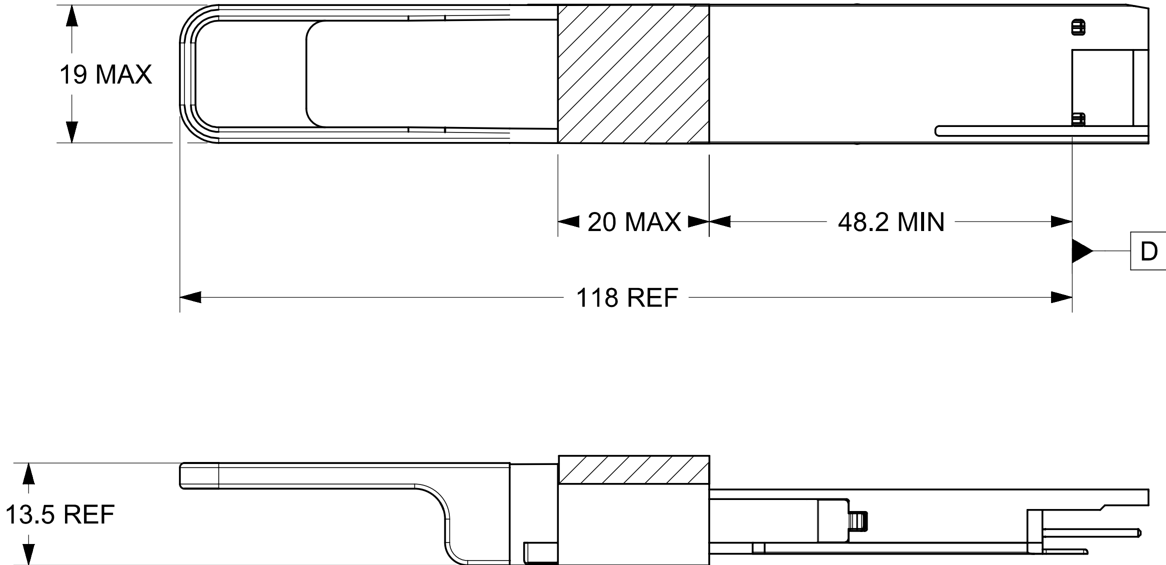


Figure 94: Informative overall module length with handle for Type 1 module

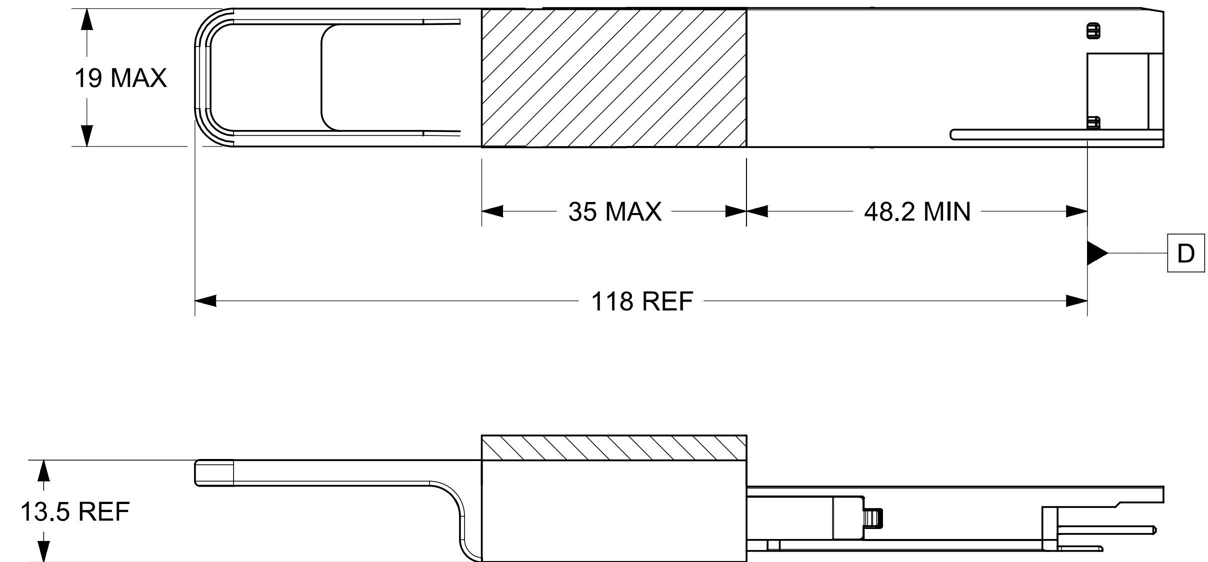


Figure 95: Informative overall module length with handle for Types 2A, 2B, and 2C modules

The elastomeric handle should not interfere with the optical plugs used in Section 5.2.

Appendix C Informative module heat sink Type 2A, 2B, 2C examples

This appendix contains several designs examples of higher power Type 2A, 2B, and 2C QSFP-DD/QSFP-DD800/QSFP-DD1600 with integrated nose heat sinks.

Thermal design is system dependent; however, systems seeking to maximize the benefit of the external heat sink of Type 2A, 2B, and 2C modules should consider minimizing bypass of airflow through the external heat sink. Type 2A, 2B, and 2C modules have a heatsink on the nose of the module. The QSFP-DD800 type 2B modules are taller and can only be used in QSFP-DD800 stack cages as the ports on a stacked QSFP-DD800 cage are separated by 1.7 mm more than QSFP-DD cages in section 6.7. The QSFP-DD1600 type 2C modules are taller and can only be used in QSFP-DD1600 stack cages as the ports on a stacked QSFP-DD800 cage are separated by 1.87 mm more than QSFP-DD800 cages 7.5. However, a Type 2A module can be used in all hosts and Type 2B module can be used with QSFP-DD800 and QSFP-DD1600 hosts.

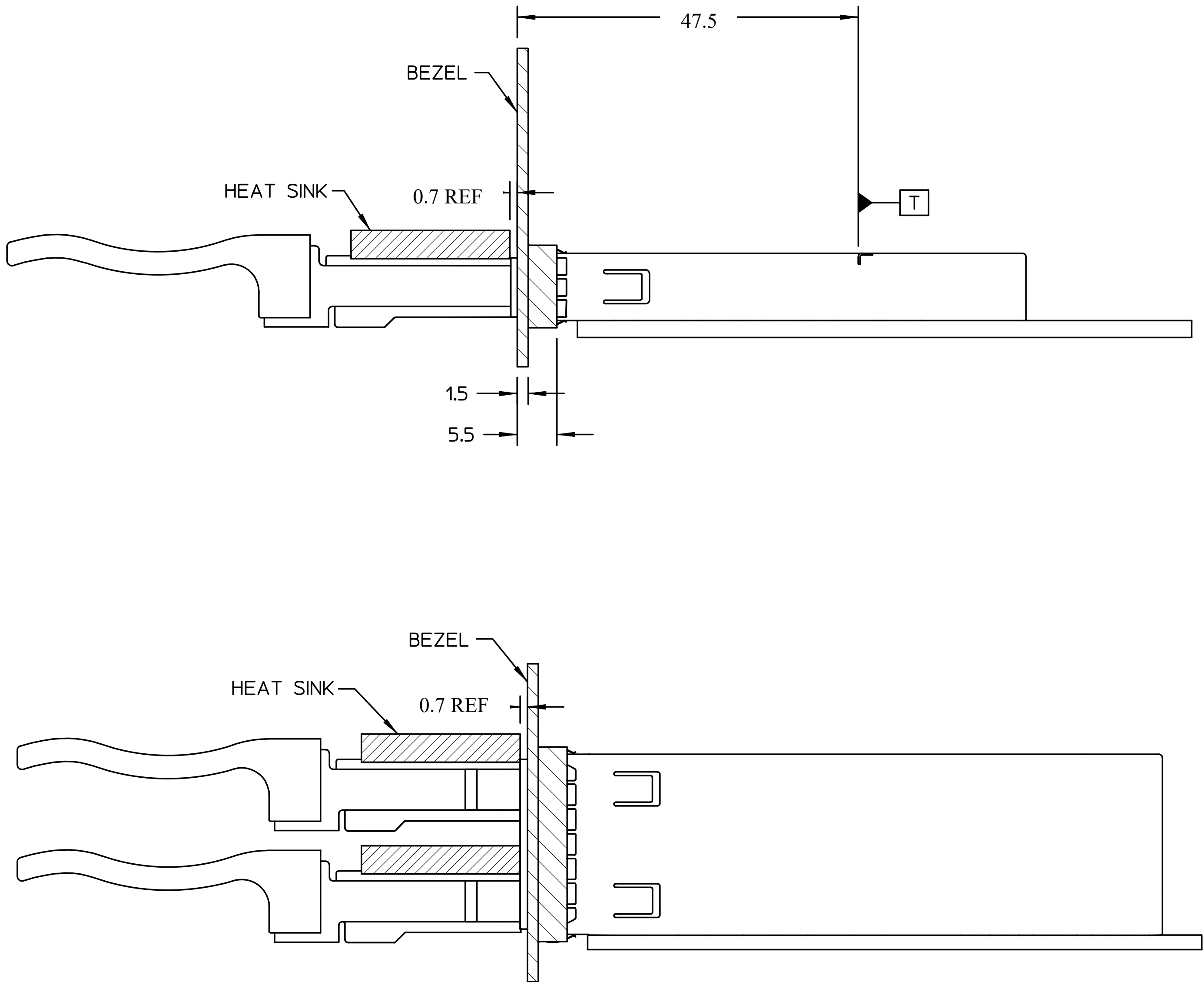
One potential method is to use a minimal gap between the outer surface of the front panel and the trailing edge of the external heat sink fins as shown in this appendix. Types 2A, 2B, and 2C modules insertion are shown in Figure 96. Types 2A, 2B, and 2C examples of 1X1 bezel design are shown in Figure 97. Example of 2X1 bezel design is shown in Figure 98. Type 2A, and Type 2B extruded heat sink examples are shown in Figure 99. Type 2A and Type 2B die cast heat sinks with metal cover examples are shown in Figure 100. Type 2A and Type 2B zipper fin heat sink examples are shown in Figure 101.

Dimensions A, B, and C for Type 2A, 2B, and 2C heat sinks in Figure 98, Figure 99, Figure 100, and Figure 101 are given in Table 24. All dimensions shall have dimension tolerance of +/-0.1 mm.

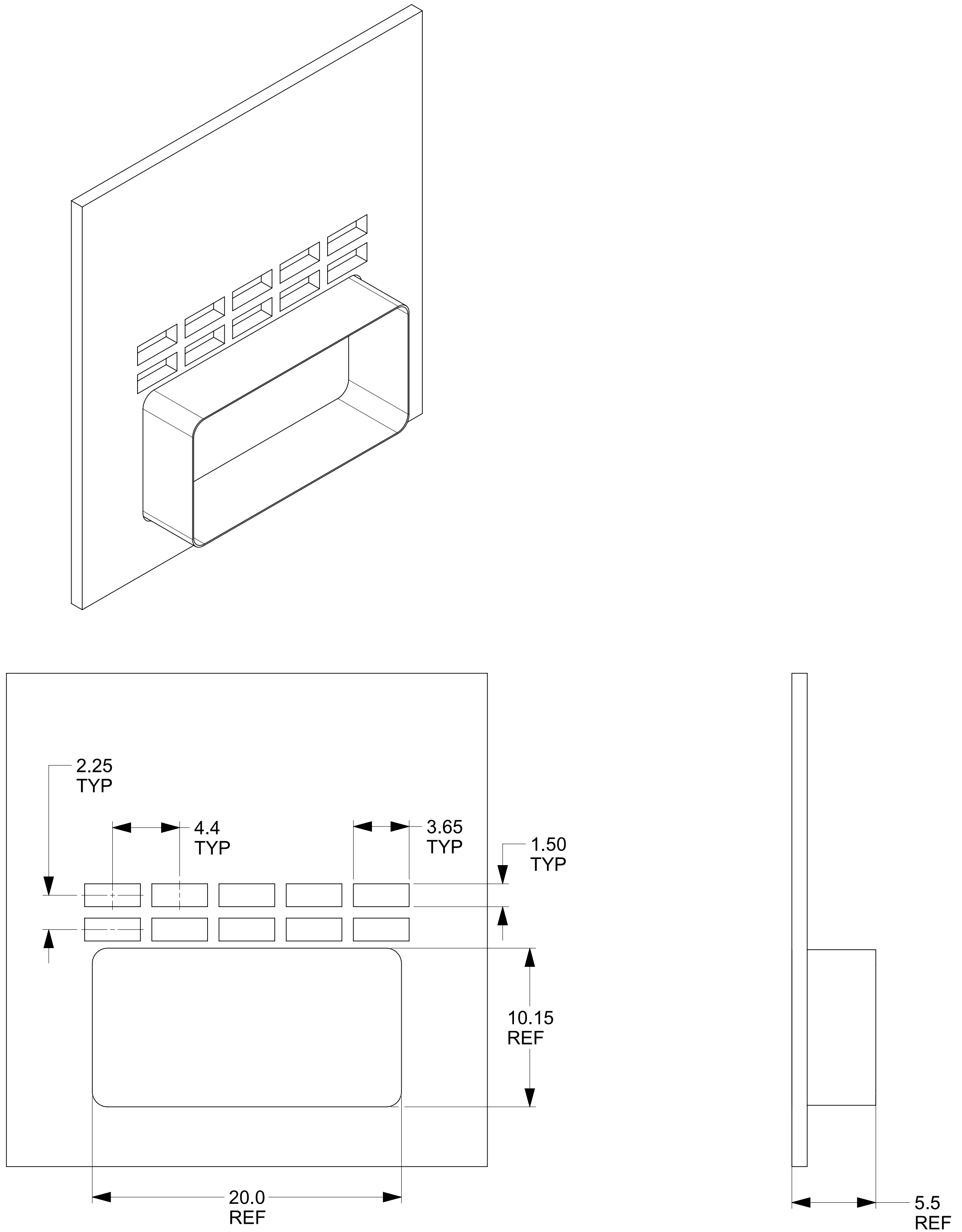
Table 24- Dimensions for QSFP-DD/QSFP-DD800/QSFP-DD1600 and Module Type 2A, 2B, and 2C

Module Type	Dimension A
QSFP-DD	25.7 mm
QSFP-DD800	27.83 mm
QSFP-DD1600	29.70 mm

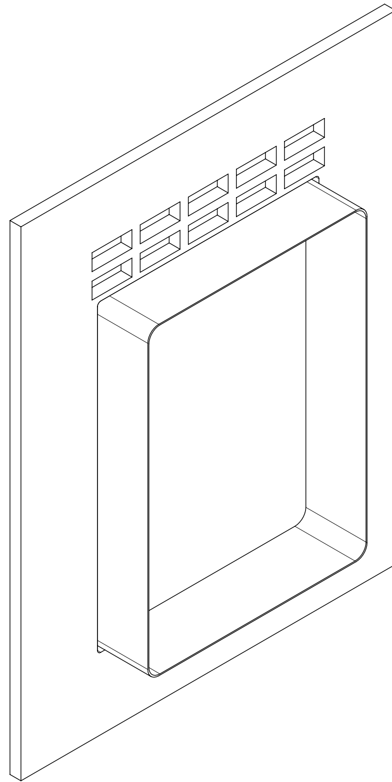
Dimensions	Module Type 2A	Module Type 2B	Module Type 2C
B (max)	3.4 mm	5.1 mm	6.91 mm
C (REF)	13.5 mm	15.2 mm	17.00 mm



1
2
3 **Figure 96: Example of single and dual stacked QSFP-DD/QSFP-DD800/QSFP-DD1600 module insertions**
4
5



1
2 **Figure 97: Types 2A, 2B, 2C example of 1X1 bezel design**
3
4



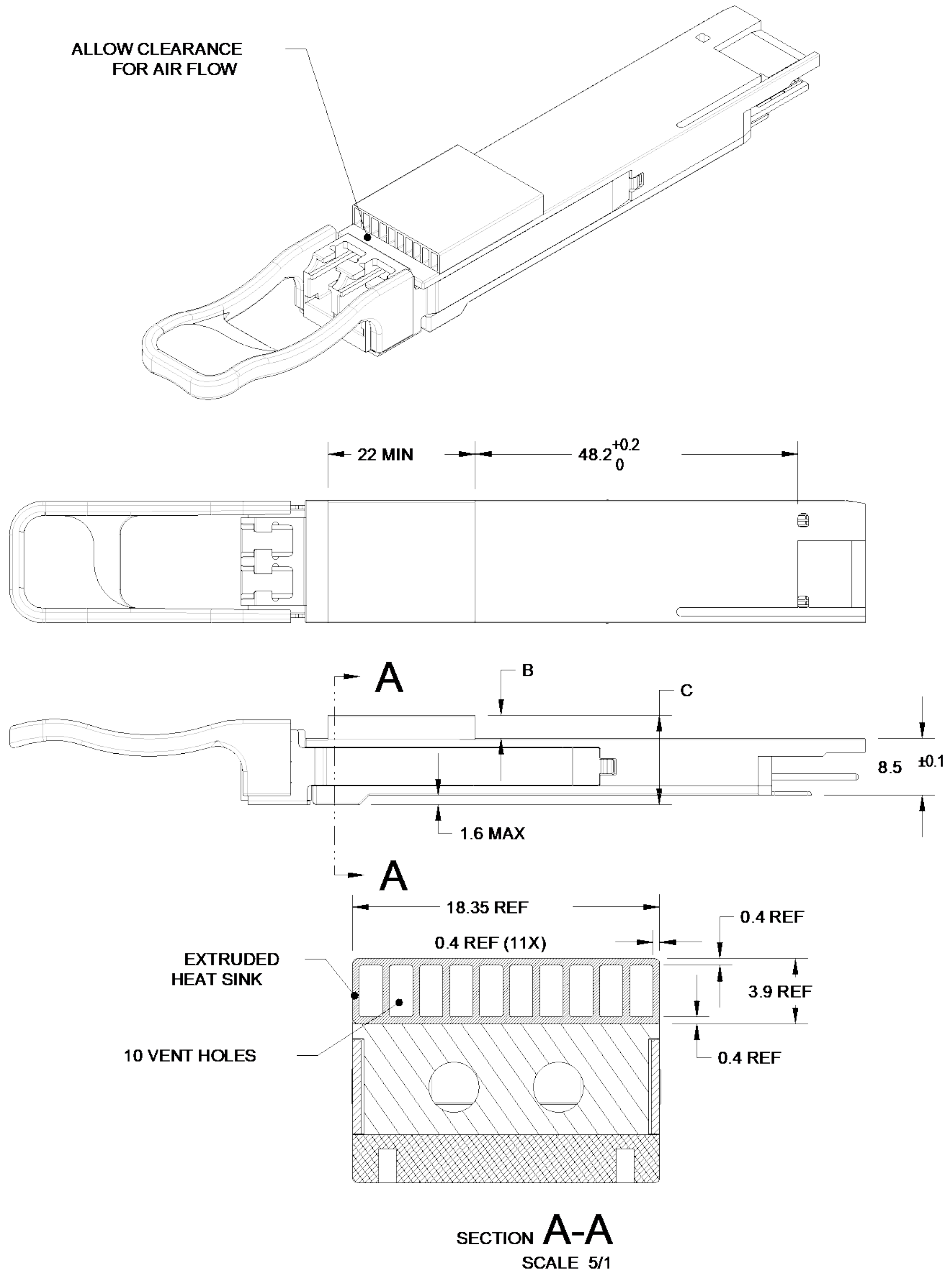
OPTIONAL BEZEL CUTOUTS
FOR AIR FLOW ARE SHOWN
FOR REFERENCE
QUANTITY AND SIZE OF CUTOUTS
ARE NOT DEFINED BY THIS SPECIFICATION

A

R0.3 REF
TYP

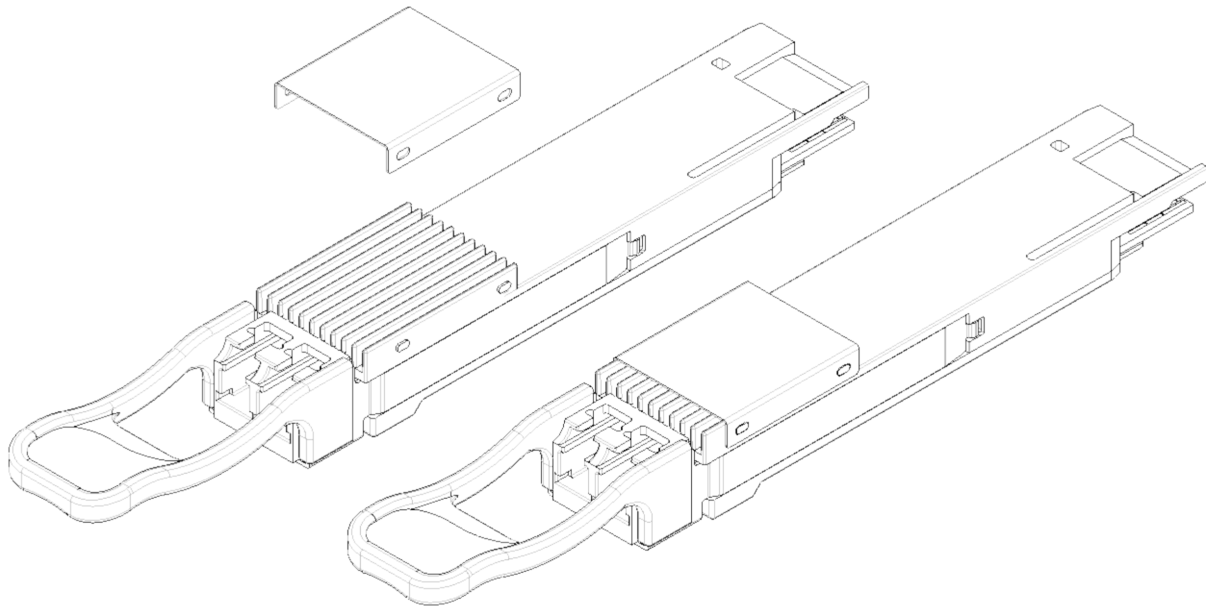
20.0
REF

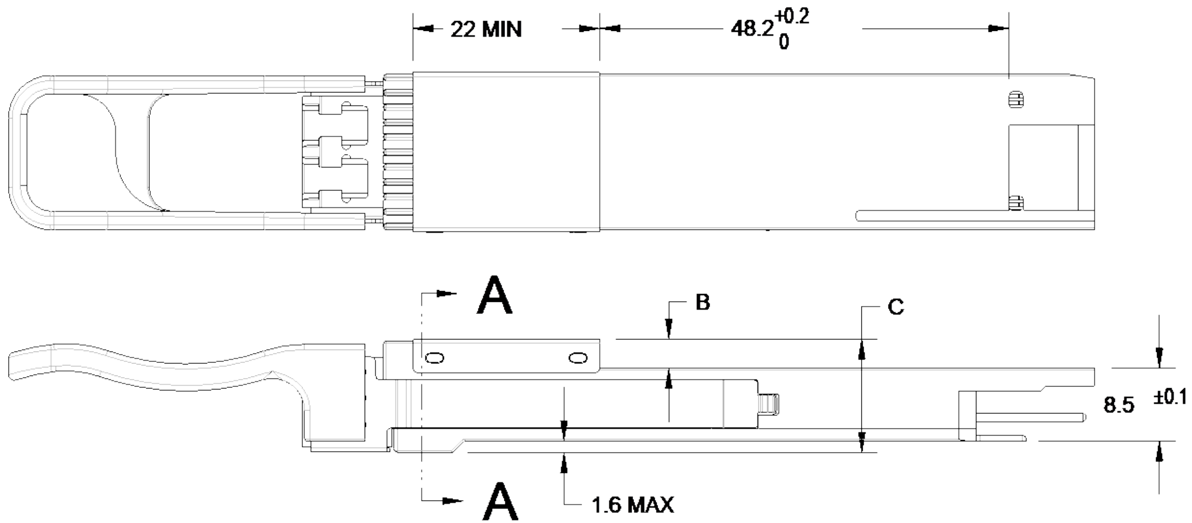
Figure 98: Type 2A, 2B, 2C example of 2X1 bezel design

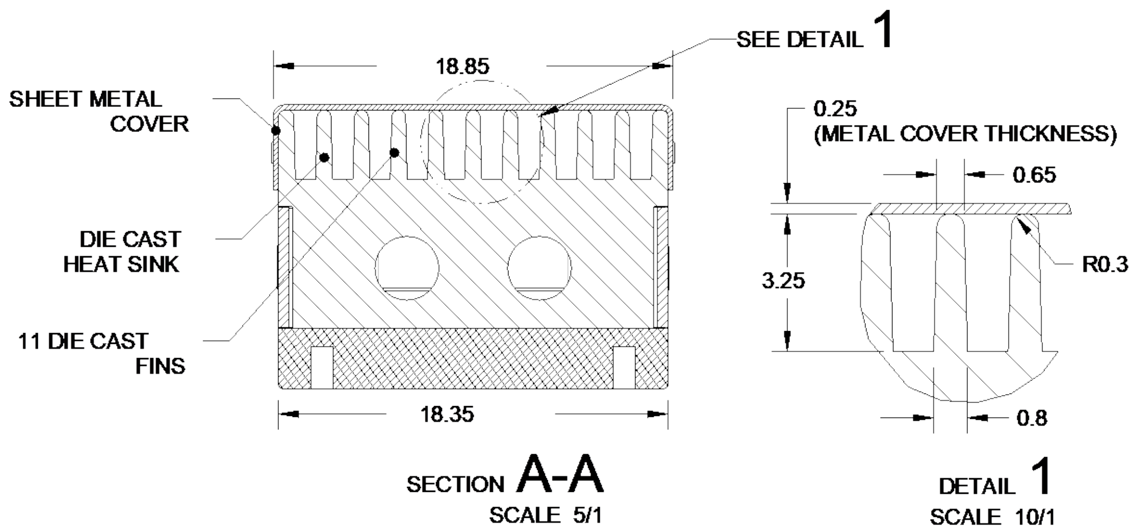


1
2 **Figure 99: Example of extruded Heat Sink**

1

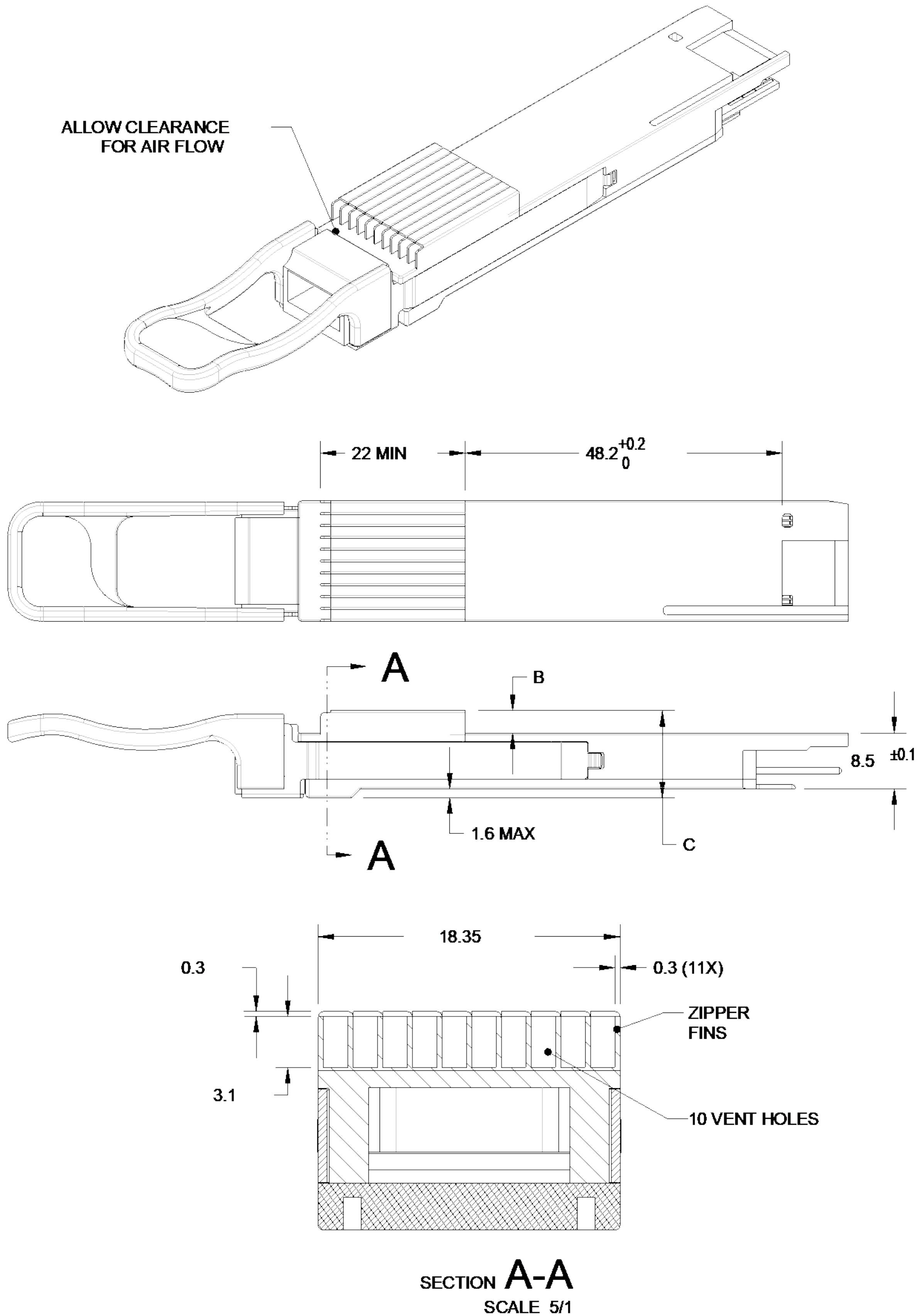






2
3 **Figure 100: Example of die Cast Heat Sink with Metal Cover**

1



2
3 **Figure 101: Example of zipper Fin Heat Sink**

Appendix D QSFP-DD800 Cage and Heat Sink Mechanism and EMI fingers

This Annex details is an optional QSFP-DD800 compliant cage design which can provide improved EMI and thermal performance. Implementation of this option does not require a change to the host PCB layout, front panel cutout or the module.

D.1 Introduction

The QSFP-DD800 cage design is an integral element of the EMI and thermal design strategy in QSFP-DD800 based architectures. In this annex a cage design is described with features specifically targeting these design elements. The key features are as follows:

a) A dual row EMI spring clip which has been shown to enhance the shielding performance of the cage
b) A heat sink attach mechanism which has been shown to enhance the heat dissipation properties of the module when inserted into the cage.

D.2 EMI Spring Clip Mechanical Definition

Figure 102 illustrates the connection of the transceiver to the front panel using a dual contact EMI spring clip. The additional connection provided by path #2 in Figure 102 serves to reduce the transfer impedance of this connection resulting in improved shielding performance. Figure 103 shows the detail of the EMI spring clip.

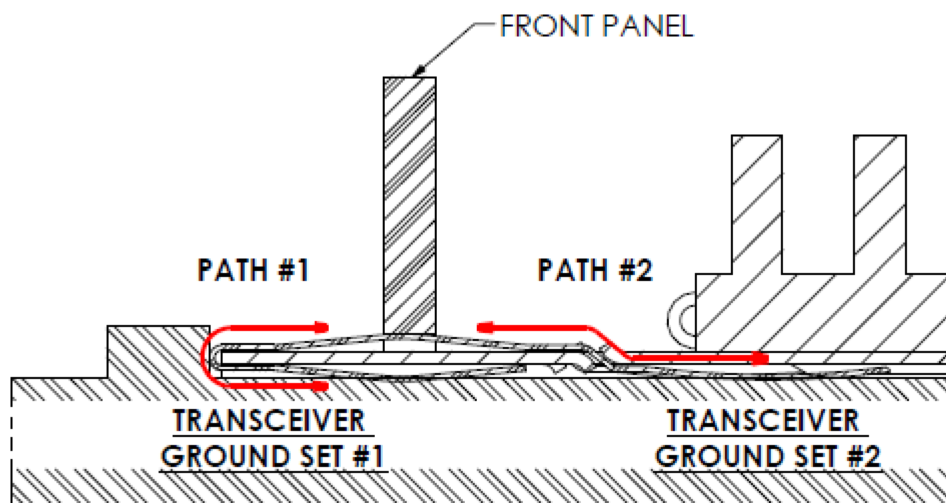


Figure 102: Dual grounding path for EMI spring clip

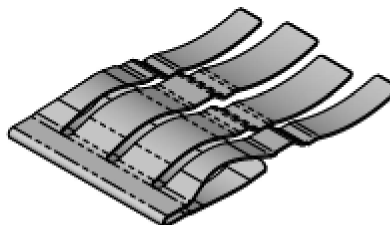


Figure 103: EMI spring clip

D.3 Heat Sink Attach Mechanism

A cage and heat sink attached mechanism is shown in Figure 104 and Figure 105. This cage implementation maximizes the heat sink surface area and the corresponding module heat dissipation. This cage design relies on integrated heat sink clips at the front and rear of the cage. This approach reduces part count and allows for the use of a heat sink that is the full length of the cage. This cage design also incorporates an EMI latch shield. This optional shield covers an aperture in the cage due to the latching mechanism resulting in improved shielding performance.

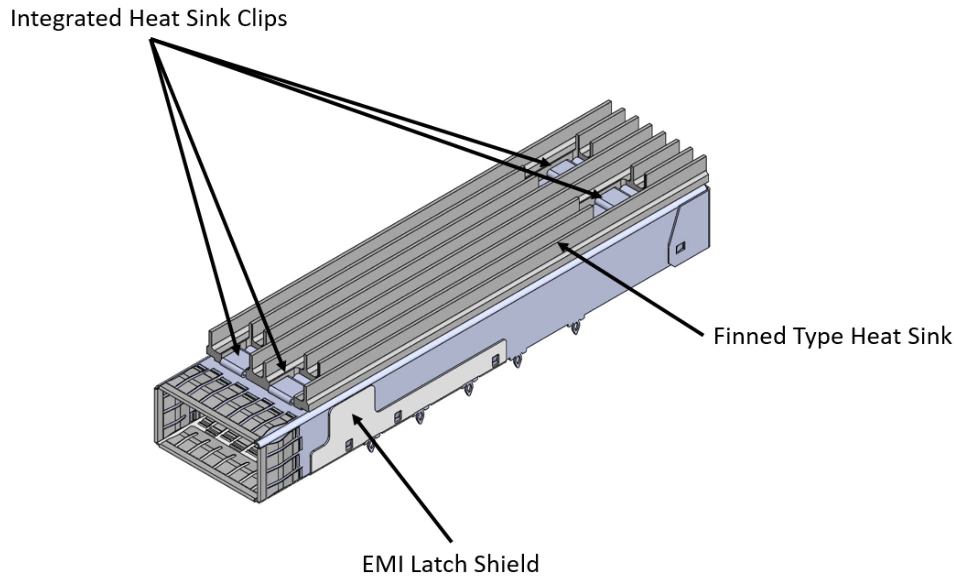


Figure 104: Cage with integrated heat sink clips and EMI latch shield

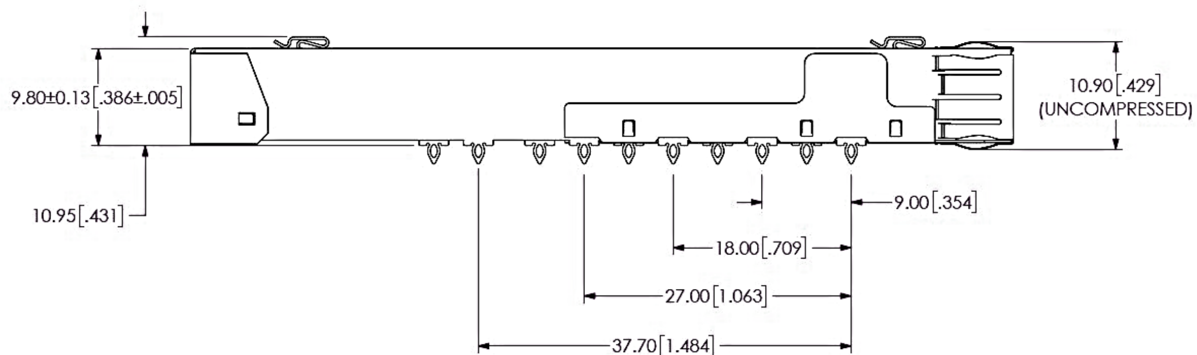


Figure 105: 1xN cage (side view)

D.4 Host PCB Layout

The features identified in this Annex do not impact the host PCB layout. Footprint compatibility permits the cage implementation in the Annex to be applied in designs with more challenging EMI and thermal objectives.

D.5 Front Panel Cutout

The EMI spring clip and cage design does not require a change to the front panel cutout allowing for mechanical design compatibility between different cage options.

Appendix E Informative QSFP-DD800 2x1 Cabled Connector and Cage

This Annex details is an optional QSFP-DD800 compliant cage design which can provide improved EMI and thermal performance. Implementation of this option does not require a change to the host PCB layout, front panel cutout or the module.

E.1 2x1 Cabled Upper Connector/Cage

The 2x1 mechanical outline for the 100 Gb/s cabled connector/cage contains an upper cabled port and a lower SMT port. The lower SMT port is identical to the 1x1 connector/cage in section 7.4. The upper connector/cage contains low speed and power contacts that are press fit to the PCB and high-speed signal contacts that are connected to cables. The cables are routed from the upper connector cage port to the host ASIC. This specification does not define the cable construction or the near ASIC connection. The connector/cage defined in this section is illustrated in Figure 106. All pluggable modules and direct attach cable plugs (Type 1, Type 2, Type 2A, and Type 2B) must mate to the connectors and cages defined in this specification.

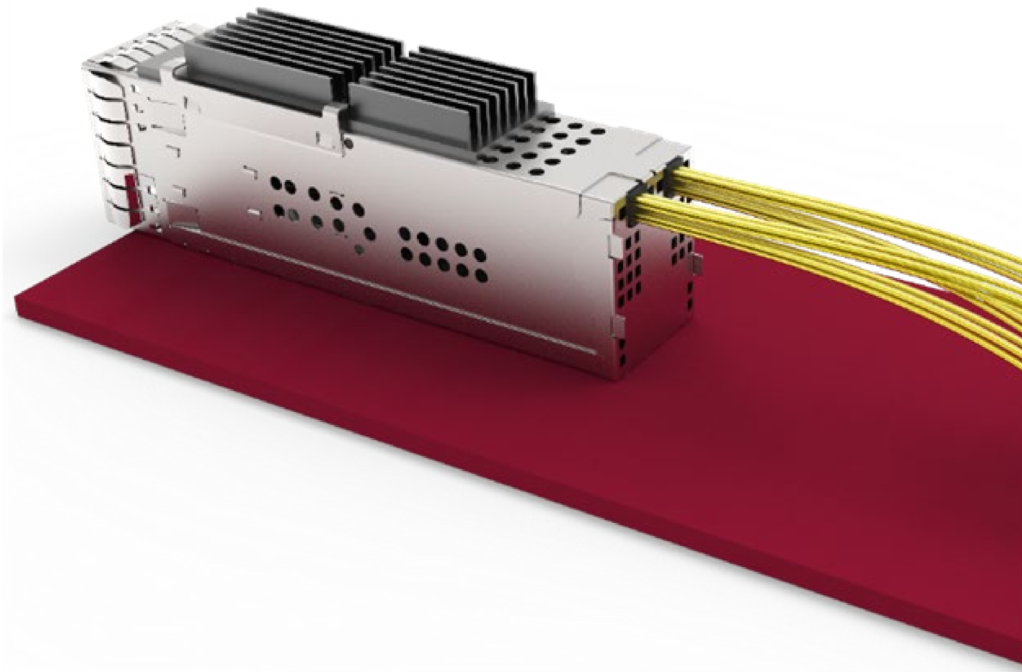


Figure 106: 2x1 Cabled upper connector/cage

E.2 2x1 cabled connector/cage Electrical Connector Mechanical

The 2x1 stacked cabled cage is illustrated in Figure 107. Figure 108 shows the stacked connector placement over the surface mount lower connector. Figure 109 shows the lower surface mount connector attached to the host PCB, the upper cabled connector and the 2x1 cage placement prior to press fit into the host PCB. Cabled cage and connector detailed drawings are shown in Figure 111 and Figure 112.

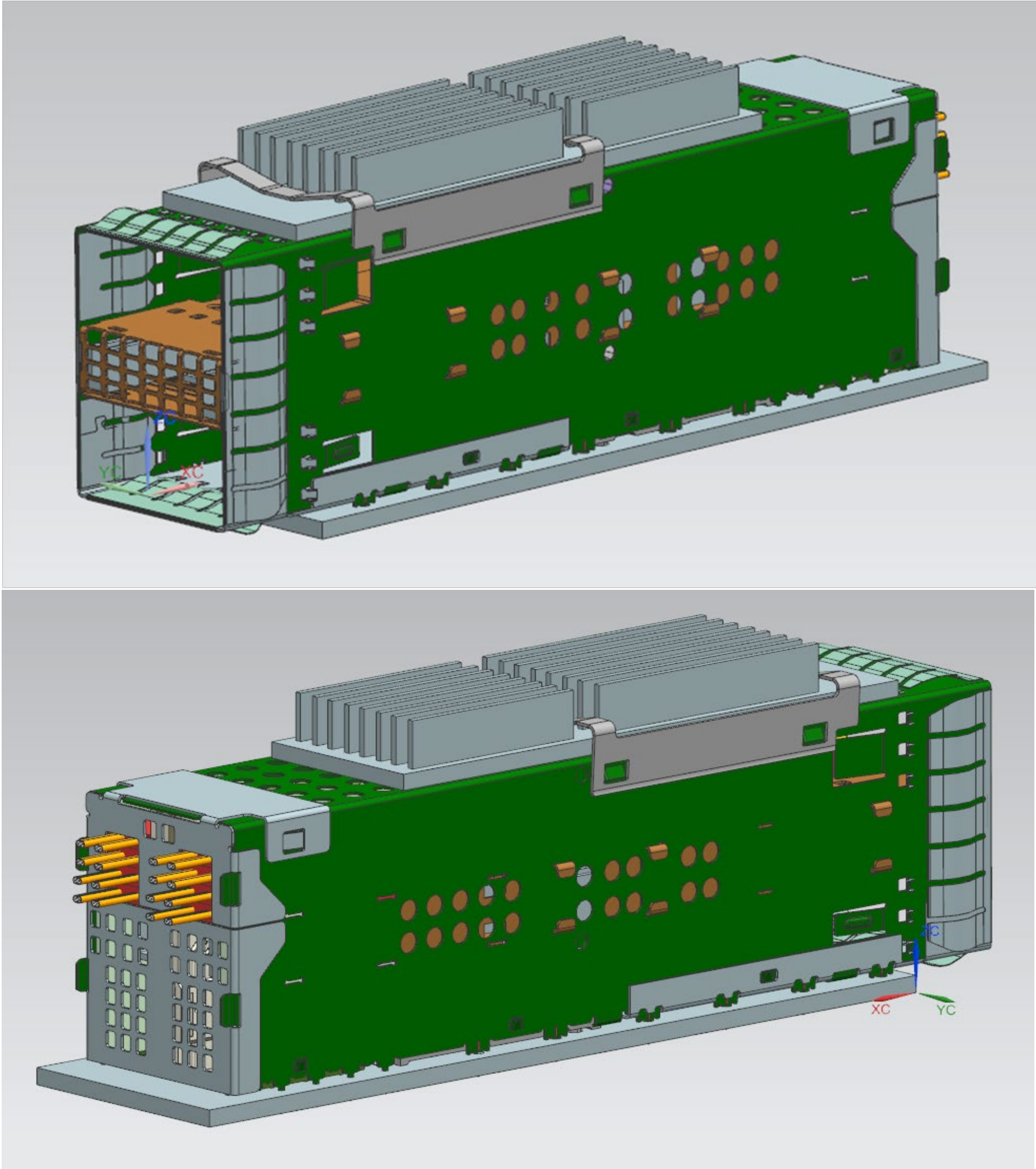
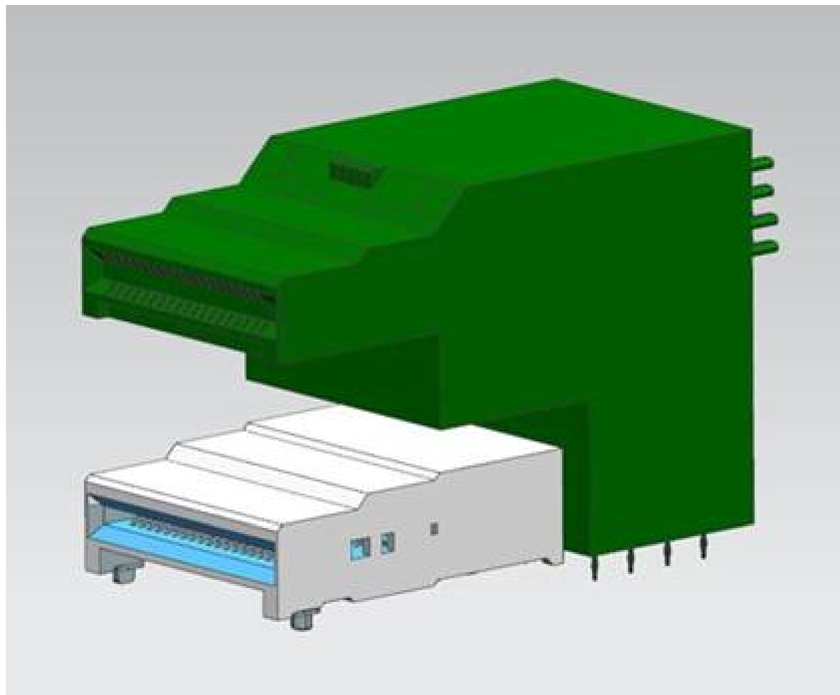


Figure 107: 2x1 Cabled upper connector/cage illustration



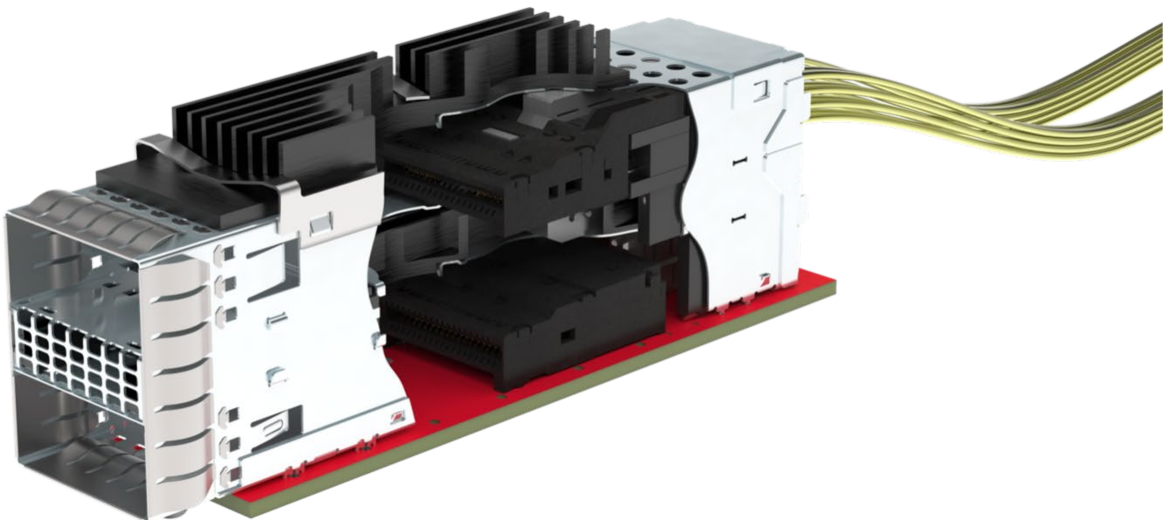
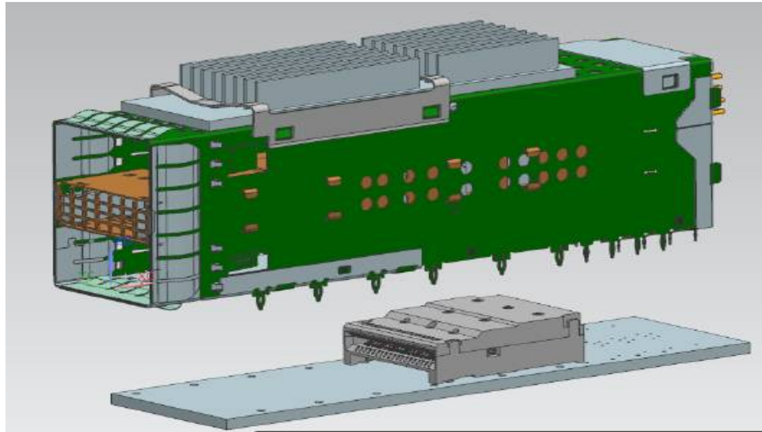


Figure 108: Cabled upper connector over existing surface mount connector



1
2 **Figure 109: Lower SMT connector, upper press fit connector, and the 2x1 cage**
3

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

△3 DIMENSIONS FROM INSIDE SURFACES OF SPRING FINGERS WHEN FULLY DEPRESSED

△4 CONNECTOR REMOVED FOR CLARITY

△5 APPLIES TO ALL SPRING FINGERS ON ALL SIDES

△6 EXTERNAL CAGE DIMENSIONS DOES, NOT INCLUDE FOLDING TABS

△7 LENGTH OF CAGE AND SIGNAL TAILS

△8 PRESS FIT CAGE PINS APPLY TO RIGHT SIDE OF CAGE

△9 PRESS FIT CAGE PINS APPLY TO LEFT SIDE OF CAGE

△10 PRESS FIT OFFSET BETWEEN RIGHT AND LEFT SIDE OF CAGE

△11 DIMENSIONS INCLUDE BACKCOVER

△12 SIZE AND POSITION OF CAGE AND CONNECTOR PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FORMAT FOOTPRINT LAYOUT

△13 CAVITY FOR HEATSINK IS OPTIONAL

△14 CONTACT PIN DIMENSION MEASURED FROM DATUM T

△15 CONTACT PIN DIMENSION MEASURED FROM DATUM T1

4
5

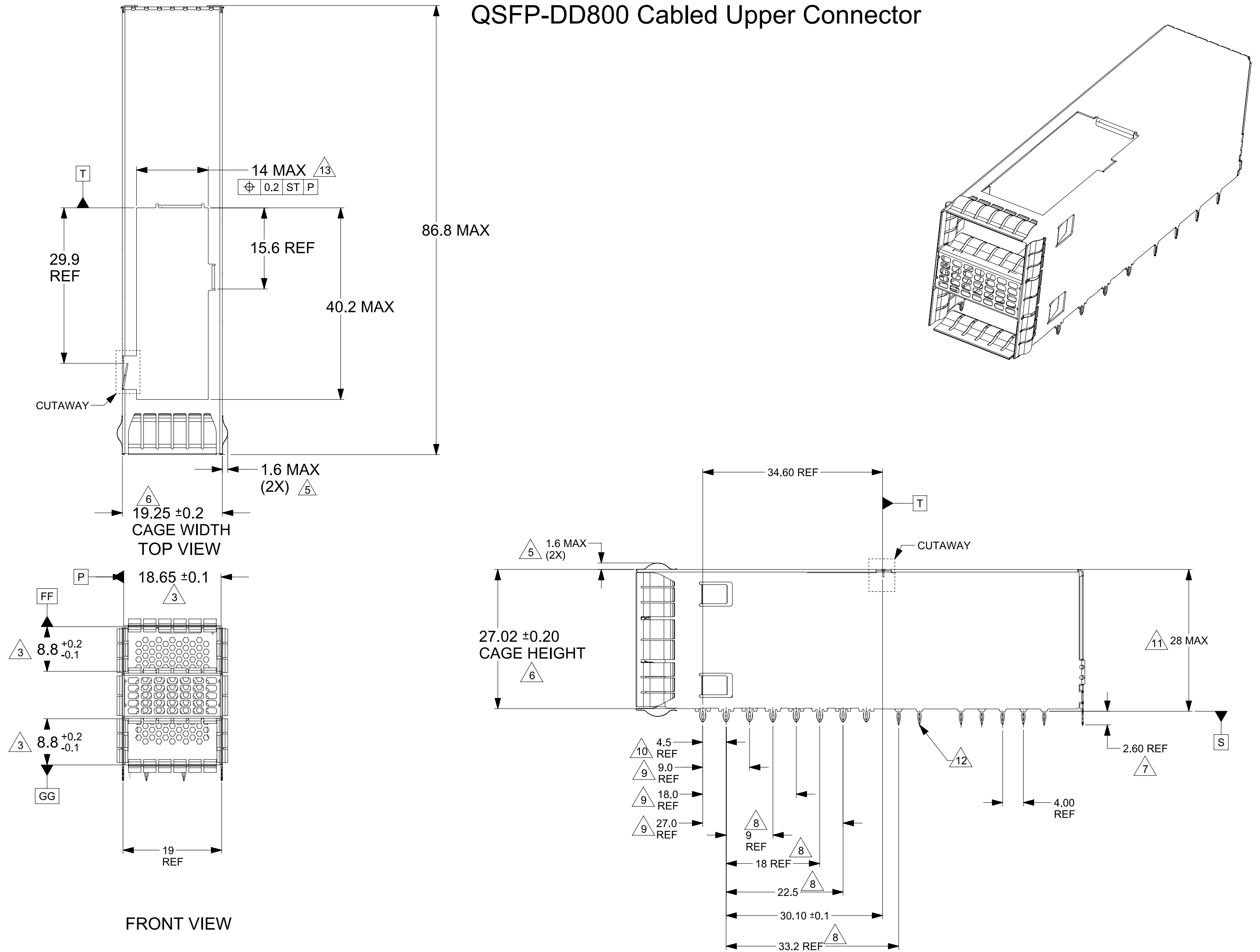
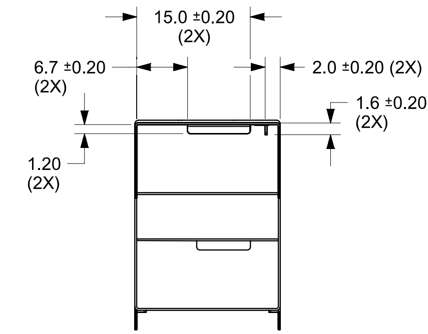
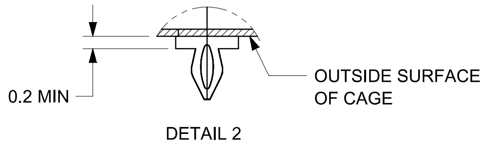
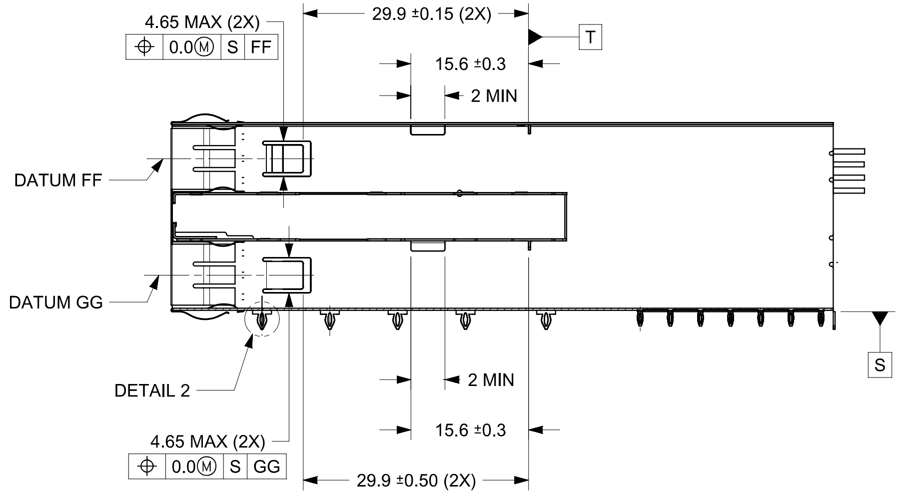
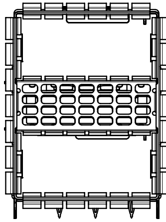


Figure 110: 2x1 Cabled over SMT connector and cage - Top View









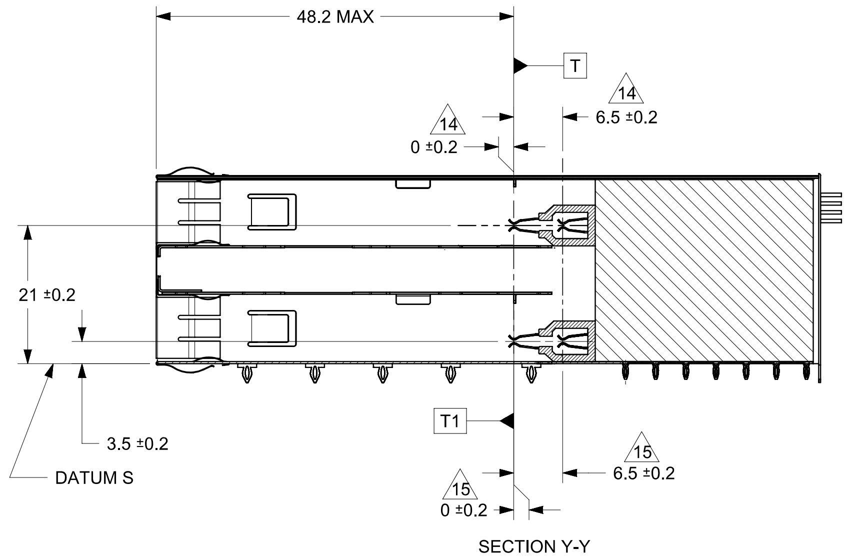
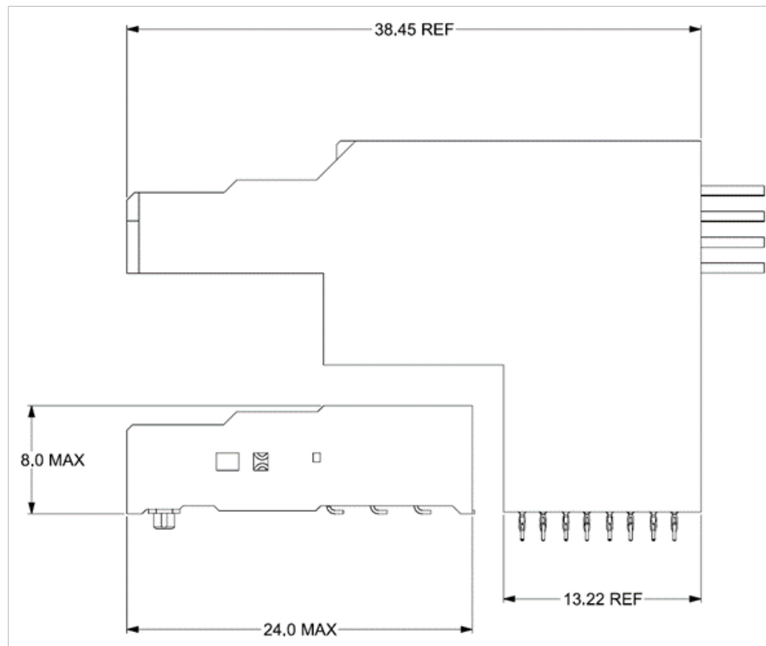


Figure 111: 2x1 Cabled over SMT connector and cage – Side View



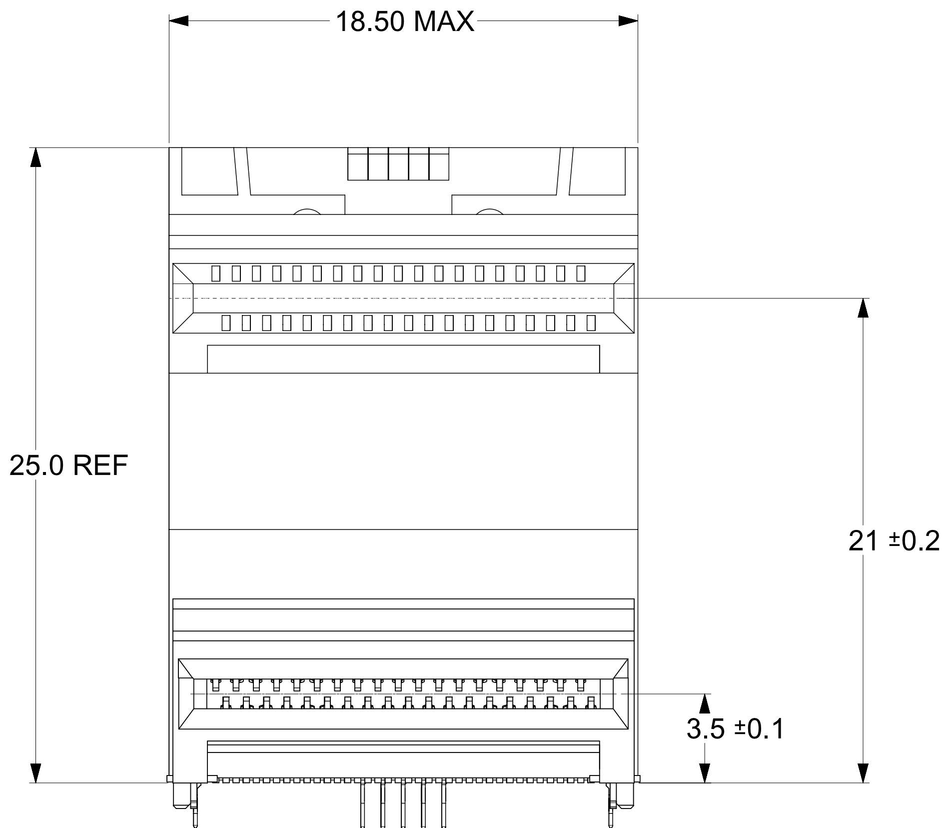


Figure 112: Cabled upper connector and surface mount connector dimensions

1
E.3 2x1 Cabled Connector and Cage host PCB layout

2 A typical host board mechanical layout for attaching the QSFP-DD800 2x1 stacked cabled Connector and
3 Cage system is shown in Figure 113, however this is only a recommendation. The location of the pattern on
4 the host board is application specific. To achieve 112 Gbps performance pad dimensions and associated
5 tolerances must be adhered to and attention paid to the host board layout. The upper QSFP-DD800 cabled
6 non high-speed contacts are press fitted into host board as shown in Figure 113, for low speed signals and
7 Gnd/Vcc contact mapping see Figure 2. Cage system ground and power must be provided through the press-
8 fit pins or dedicated cable power delivery and not through the cable shield.
9
10 Host PCB requirements notes:

1 THE ENTIRE AREA UNDER THE CONNECTOR (INSIDE DOTTED BOX) IS TO BE CONSIDERED A KEEP OUT AREA FOR COMPONENTS.

⚠2 HATCHED AREAS REPRESENT ZONES ON THE PCB THAT COME IN CONTACT WITH OR ARE CLOSE PROMIMITY TO THE PLASTIC HOUSING OR THE CONNECTOR CAGE. INDICATED AREAS TO BE CONSIDERED TRACE FREE.

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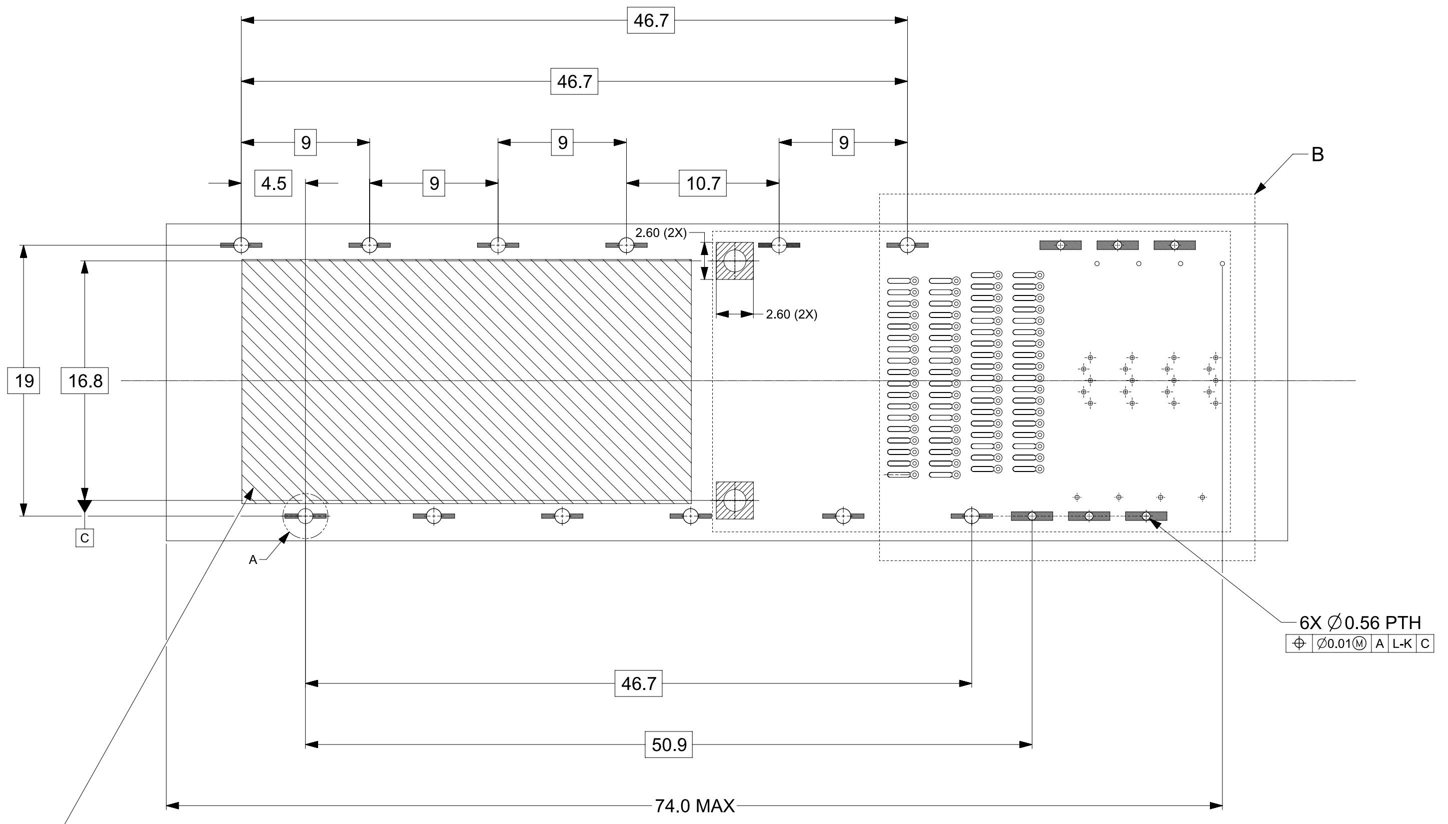
12



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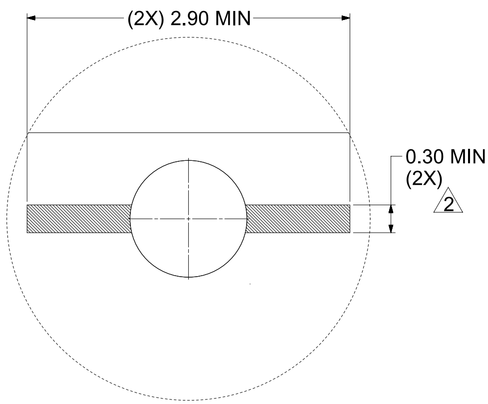

2
3
4 **Figure 113: 2x1 Cabled upper connector/cage host board connector contacts**
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Appendix F QSFP-DD1600 mechanical enhancements for high power modules

The thermal performance of the QSFP-DD1600 module can be improved with some additional mechanical features to the nose heatsink, to the bottom of the QSFP-DD1600 module case and to the host PCB. These module and host modifications are optional but recommended for any designs expected to be above 20 W.

To increase the airflow along the bottom side of the module, the host PCB can be notched allowing airflow through the faceplate to reach a bottom riding heatsink. Additional recessed channels on the QSFP-DD1600 module case bottom allow the bypass of the airflow around the module body.

QSFP-DD1600 module mechanical is based on QSFP-DD800 mechanical in section 7.2, based drawing shown in Figure 63 and Figure 64. QSFP-DD1600 improved module latch pocket is shown in Figure 78 and the module leading edge Detail 1 shown in Figure 79. QSFP-DD1600 optional thermally improved design is based on additional heat exchange on the module bottom surface with improved module nose heat sink as shown in Figure 114, Figure 115, Figure 116, and Figure 117.

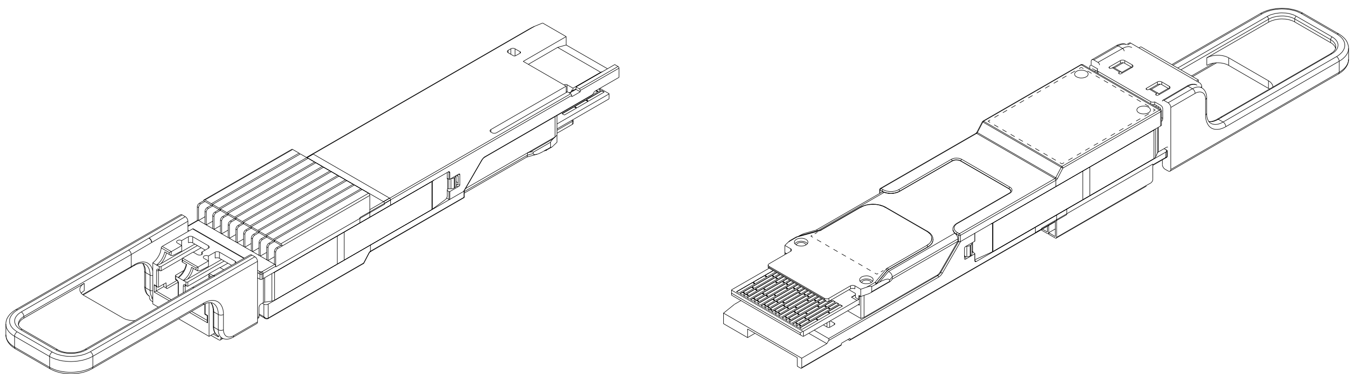
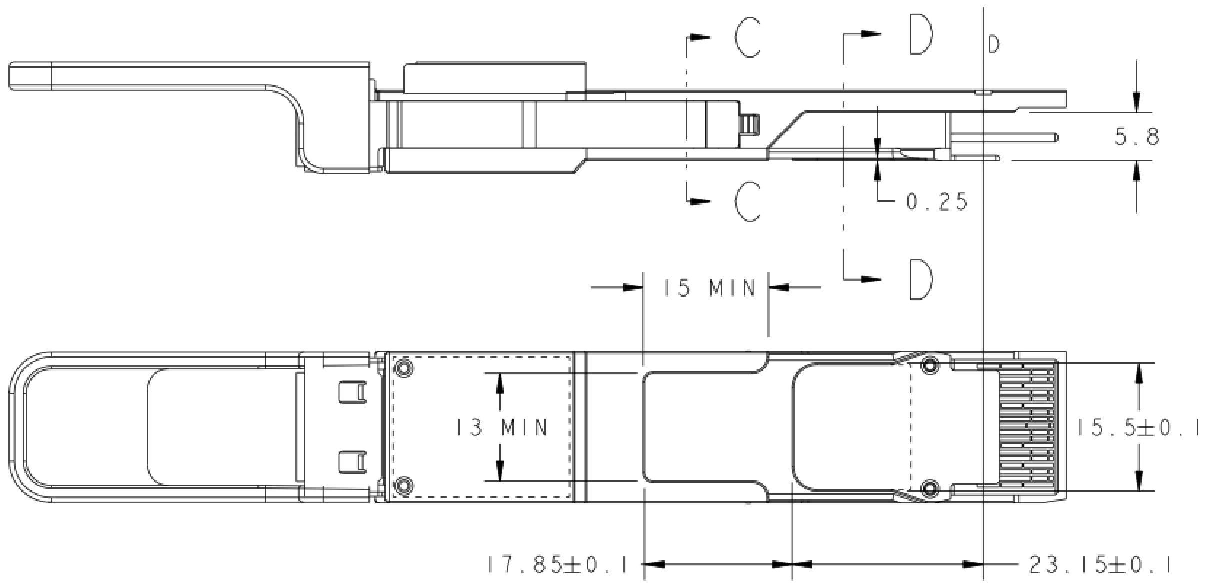


Figure 114: QSFP-DD1600 Improved thermal design top/bottom module views



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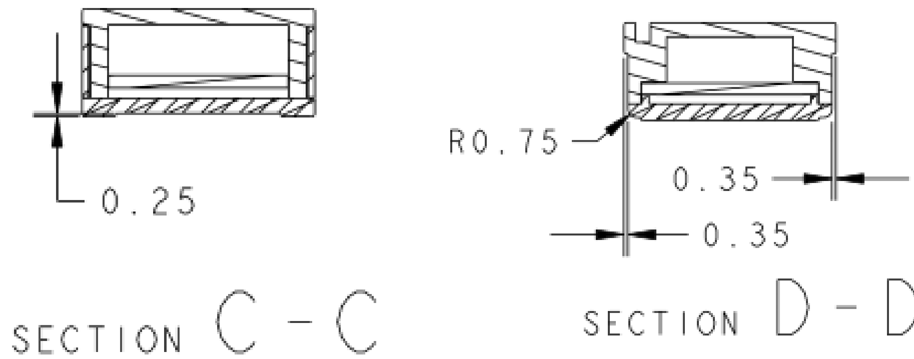

2
3
4 **Figure 115: QSFP-DD1600 Improved thermal design module (bottom and sides views details)**
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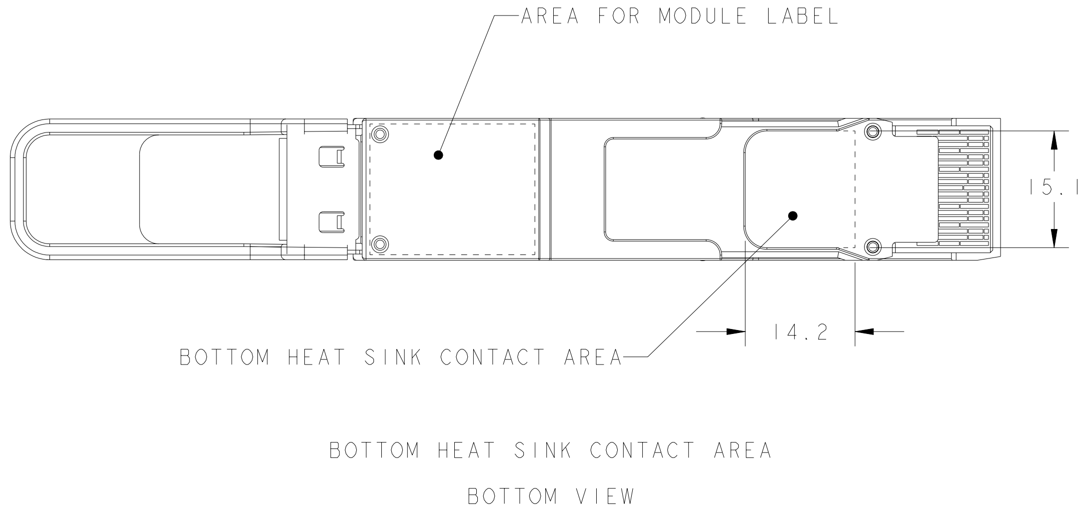

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2 **Figure 116: QSFP-DD1600 Module improved thermal design (bottom heat sink contact)**
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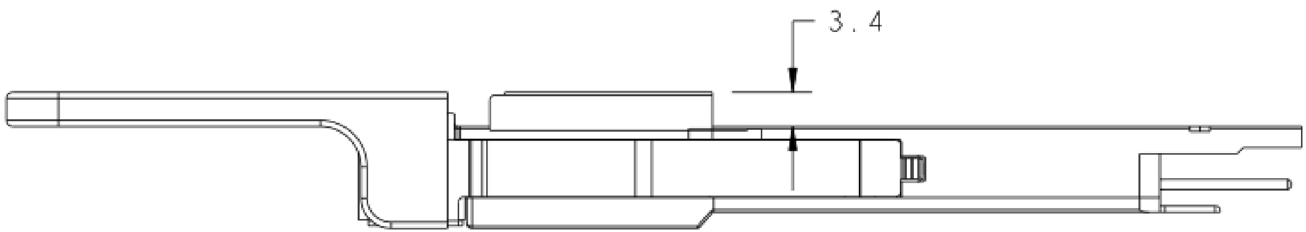

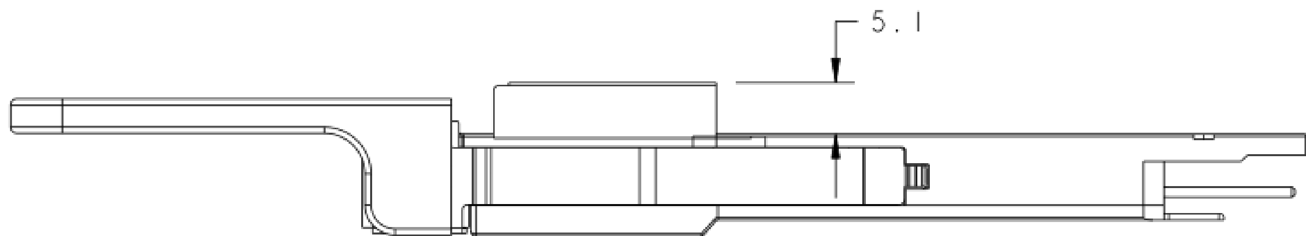

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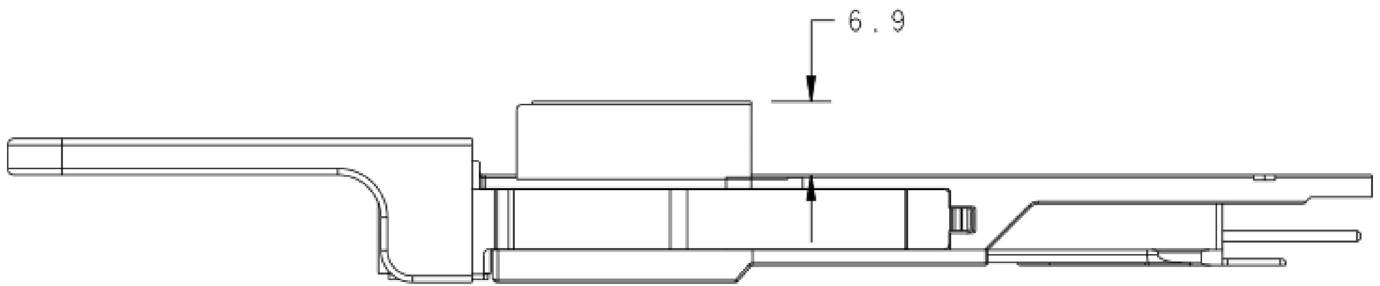

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8 **Figure 117: QSFP-DD1600 Improved module thermal design (types 2A, 2B, and 2C)**
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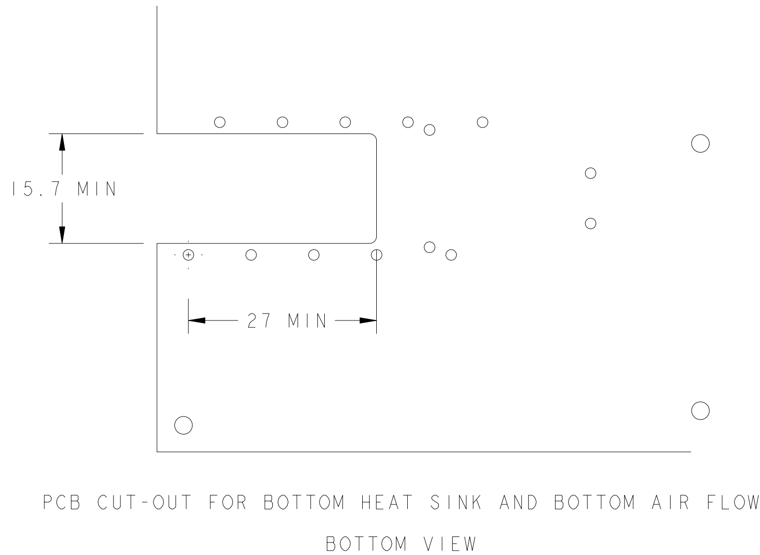
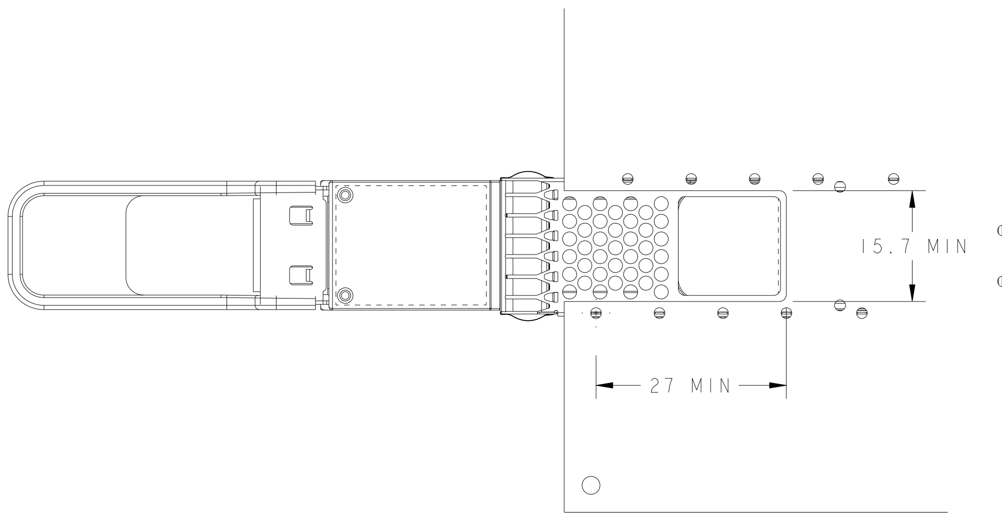
1
F.1 QSFP-DD1600 Thermally enhanced PCB cutout

2 The QSFP-DD thermal improved design module requires additional features at PCB design described in Figure
3 118 and at cage design described in Figure 119.
4



5
6 **Figure 118: QSFP-DD1600 Improved module thermal design (PCB cut out requirement)**



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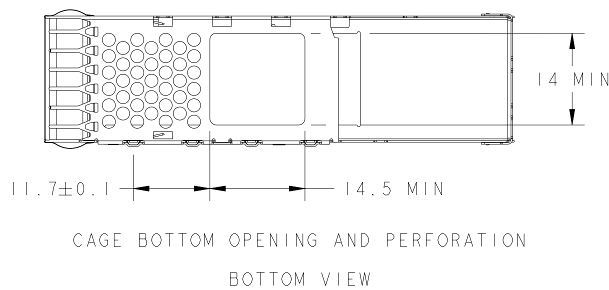

8
9 **Figure 119: QSFP-DD1600 Improved module thermal design (bottom cage opening)**

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