Q-100G-AOCxM

100G QSFP28 to QSFP28 Active Optical Cable (AOC), 1~100 meters

Features

- Hot-pluggable QSFP28 form factor
- 4 high-speed full duplex channels
- Supports 103.1Gb/s aggregate bit rate
- 4x25Gbps 850nm VCSEL laser
- QSFP28 MSA SFF-8636 compliant
- Low power dissipation:<2.5W per cable end
- Available in lengths of 1 to 100 meters
- RoHS-6 compliant
- Operating temperature range: 0 to 70°C

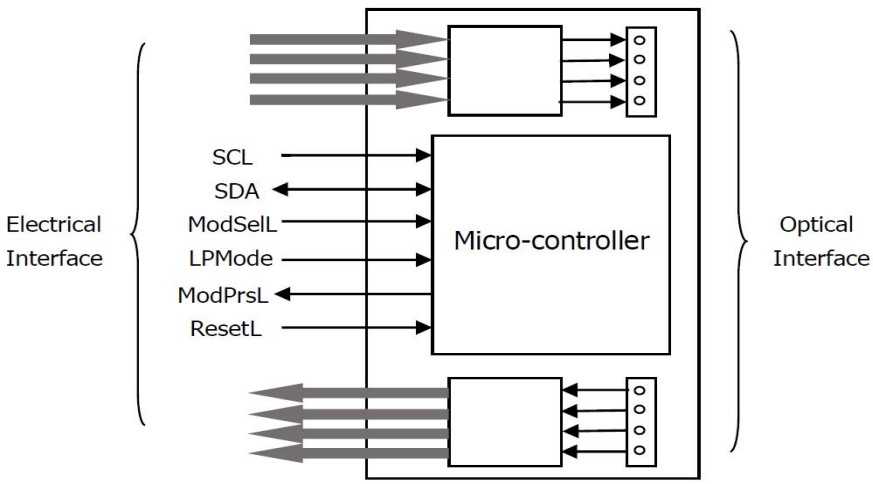
Applications

- 100 Gigabit Ethernet links
- Infiniband EDR interconnects
- Data center cabling infrastructure
- High density connections between networking equipment

Description

Optcore's Q-100G-AOCxM family is QSFP28 4-channel active optical cables (AOC) for 100G Ethernet (100GbE) and Infiniband EDR Applications. This full-duplex optical assembly offers four independent transmit and receive channels, each capable of up to 25Gbps for an aggregate bandwidth of 100Gbps. The 100G QSFP28 AOC cables can be used as a direct replacement for traditional QSFP28 DAC (direct attach copper cables) and QSFP28 transceivers of short reach while providing lighter weight, improved signal integrity, lower cost, and performance value. The optical end is never exposed to a data center environment and therefore does not require cleaning or special handling. They are designed for high speed, high density, and low power consumption for today's data center networking applications.

Block Diagram



The 100G QSFP28 AOC cable has a miniature optical engine embedded into each end of the cable assembly. The

engines interconnect four independent transmit/receive lanes. A functional block diagram of the engine is shown in the above Figure. The transmitter sections consist of a 4-channel VCSEL array, a 4-channel input buffer, and a laser driver.

An onboard micro-controller provides control, diagnostic, and monitoring for the cable functions and the external I2C serial communication interface. The Receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Maximum Supply Voltage	Vcc	-0.5	4.0	V	
Storage Temperature	T_S	-40	85	°C	
Operating Humidity	RH	5	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.13	3.3	3.47	V	
Power Supply Current	Icc			750	mA	
Power Dissipation	Pm			2.5	W	
Case Operating Temperature	Tc	0		70	°C	
Data Rate			25.78		Gbps	Each channel
Bit Error Rate	BER			10^{-12}		
Fiber Bend Radius	Rb	3			cm	

Optical and Electrical Characteristics

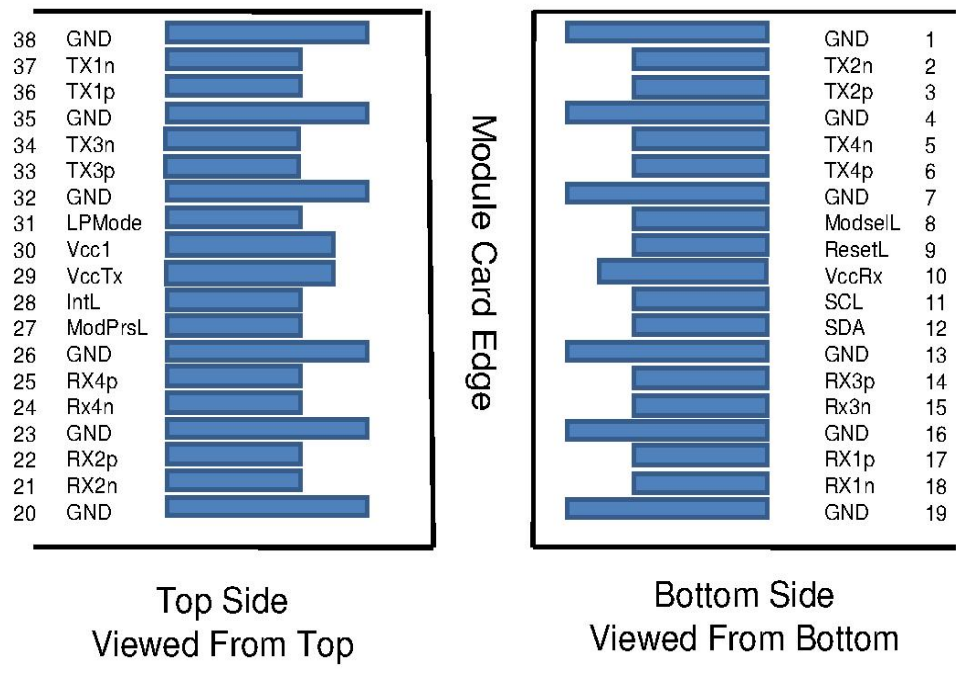
Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate, each lane	DRpl	Gb/s	25.78125 ±100 ppm			1
Center Wavelengthe	λ	nm	840	850	860	
RMS Spectral Width		nm		0.6		
Average launch power, each lane	Pavg	dBm	-8.4		2.4	
Optical modulation amplitude, each lane (OMA)	OMA	dBm	-6.4		3	
Extinction ratio	ER	dB	2			
Average Launch Power of OFF Transmitter, per Lane	RIN	dBm			-30	
Encircled Flux	FLX	dBm	>86% at 19 um <30% at 4.5 um			
Optical return loss tolerance		dB			12	
Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3}			{0.3,0.38,0.45,0.35,0.41,0.5}			2
Receiver						
Receive Rate for Each Lane	DRpl	Gb/s	25.78125 ±100 ppm			3
Four Lane Wavelength Range	λ	nm	840		860	

Overload Input Optical Power	Pmax	dBm	3.4			
Average Receive Power for Each Lane	Pin	dBm	-10.3		2.4	4
Receiver Sensitivity(OMA)per lane	Psens	dBm			-5.2	
Recevier Reflectance	Rfl	dB			-12	
Receiver Eye MaskDefinition {X1, X2, X3, Y1, Y2,Y3}		{0.28,0.5,0.5,0.33,0.33,0.4}				5
Los De-Assert	Pd	dBm			-13	
Los Assert	Pa	dBm	-30			
Loss Hysteresis	Pd-Pa	dBm	0.5			

Notes:

1. Transmitter consists of 4 lasers operating at a maximum speed of 25.78125Gb/s ±100ppm each.
2. Hit Ratio 1.5 x 10-3 hits/sample.
3. Receiver consists of 4 photodetectors operating at a maximum speed of 25.78125Gb/s ±100ppm each.
4. Minimum value is informative only and not the principal indicator of signal strength.
5. Hit Ratio 5 x 10-5 hits/sample.

Pin Description



Pin	Name	Logic	Description	
1	GND		Ground	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	10
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	10
4	GND		Ground	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	10
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	10
7	GND		Ground	1
8	ModSelL	LVTTL-I	Module Select	3
9	ResetL	LVTTL-I	Module Reset	4

10	Vcc Rx		+3.3V Power Supply Receiver	2
11	SCL	LVCMOS I/O	2-wire serial interface clock	5
12	SDA	LVCMOS I/O	2-wire serial interface data	5
13	GND		Ground	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	9
15	Rx3n	CML-O	Receiver Inverted Data Output	9
16	GND		Ground	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	9
18	Rx1n	CML-O	Receiver Inverted Data Output	9
19	GND		Ground	1
20	GND		Ground	1
21	Rx2n	CML-O	Receiver Inverted Data Output	9
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	9
23	GND		Ground	1
24	Rx4n	CML-O	Receiver Inverted Data Output	9
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	9
26	GND		Ground	1
27	ModPrsL	LVTTL-O	Module Present	6
28	IntL	LVTTL-O	Interrupt	7
29	Vcc Tx		+3.3V Power supply transmitter	2
30	Vcc1		+3.3V Power supply	2
31	LPMode	LVTTL-I	Low Power Mode	8
32	GND		Ground	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	10
34	Tx3n	CML-I	Transmitter Inverted Data Input	10
35	GND		Ground	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data	
37	Tx1n	CML-I	Transmitter Inverted Data Input	10
38	GND		Ground	1

Notes:

1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000 mA. Recommended host board power supply filtering is shown below .

3: The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly

selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4: The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

5: Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1.

Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology.

6: ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

7: IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

8: The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control

used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

9: Rx(n)(p/n) are module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards.

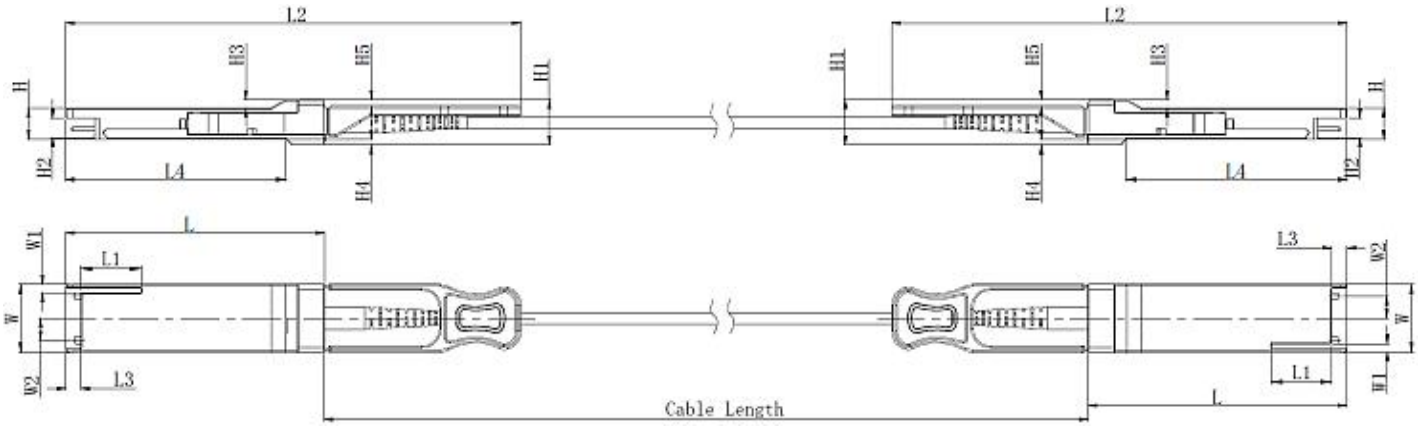
Note: Due to the possibility of insertion of legacy QSFP and QSFP+ modules into a host designed for higher speed operation, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential. Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp. In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function. For specific details refer to SFF-8636.

10: Tx(n)(p/n) are module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards. Due to the possibility of insertion of modules into a host designed for lower speed operation, the damage threshold of the module input shall be at least 1600 mV peak to peak differential. Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set. Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications,

e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended. In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function. For specific details refer to SFF- 8636.

Mechanical Dimensions

The connector is compatible with the SFF-8436 specification. *(Unit: mm)*



Mechanical Diagram, Unit mm

	L	L1	L2	L3	L4	W	W1	W2	H	H1	H2	H3	H4	H5
Max	72.2	-	128	4.35	61.4	18.45	-	6.2	8.6	12.4	5.35	2.5	1.6	2.0
Type	72.0	-	-	4.20	61.2	18.35	-	-	8.5	12.2	5.2	2.3	1.5	1.8
Min	68.8	16.5	124	4.05	61.0	18.25	2.2	5.8	8.4	12.0	5.05	2.1	1.3	1.6

Ordering information

Part number	Description
Q-100G-AOC1M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 1M
Q-100G-AOC2M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 2M
Q-100G-AOC3M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 3M
Q-100G-AOC5M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 5M
Q-100G-AOC7M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 7M
Q-100G-AOC10M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 10M
Q-100G-AOC15M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 15M
Q-100G-AOC20M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 20M
Q-100G-AOC25M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 25M
Q-100G-AOC30M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 30M
Q-100G-AOC40M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 40M
Q-100G-AOC50M	100G QSFP28 Active Optical Cable (AOC), OM3, Aqua, LSZH, 50M
Q-100G-AOC75M	100G QSFP28 Active Optical Cable (AOC), OM4, Aqua, LSZH, 75M
Q-100G-AOC100M	100G QSFP28 Active Optical Cable (AOC), OM4, Aqua, LSZH, 100M

Q-100G-AOCxxM	Customized 100G QSFP28 AOC, x:1~100 (70m@OM3, 100m@OM4) Length in meters

⚠Warnings

Process plug

The transceiver optics is supplied with a dust cover. This plug protects the transceiver optics during standard manufacturing processes by preventing contamination from air borne particles.It is recommended that the dust cover remain in the transceiver whenever an optical fiber connector is not inserted.

Handling Precautions

The transceiver optics is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety

The transceiver optics is a Class 1 laser product per international standard IEC 60825-1. Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

Appendix A. Document Revision

Version No	Date	Description
DS/V180309/EN	2018-03-09	Preliminary datasheet
DS/V211029/EN	2021-10-29	Update product image
DS/V3.0/EN	2024-08-13	Add power supply current, update power consumption and order description

For more product information, visit us on the web at www.optcore.net